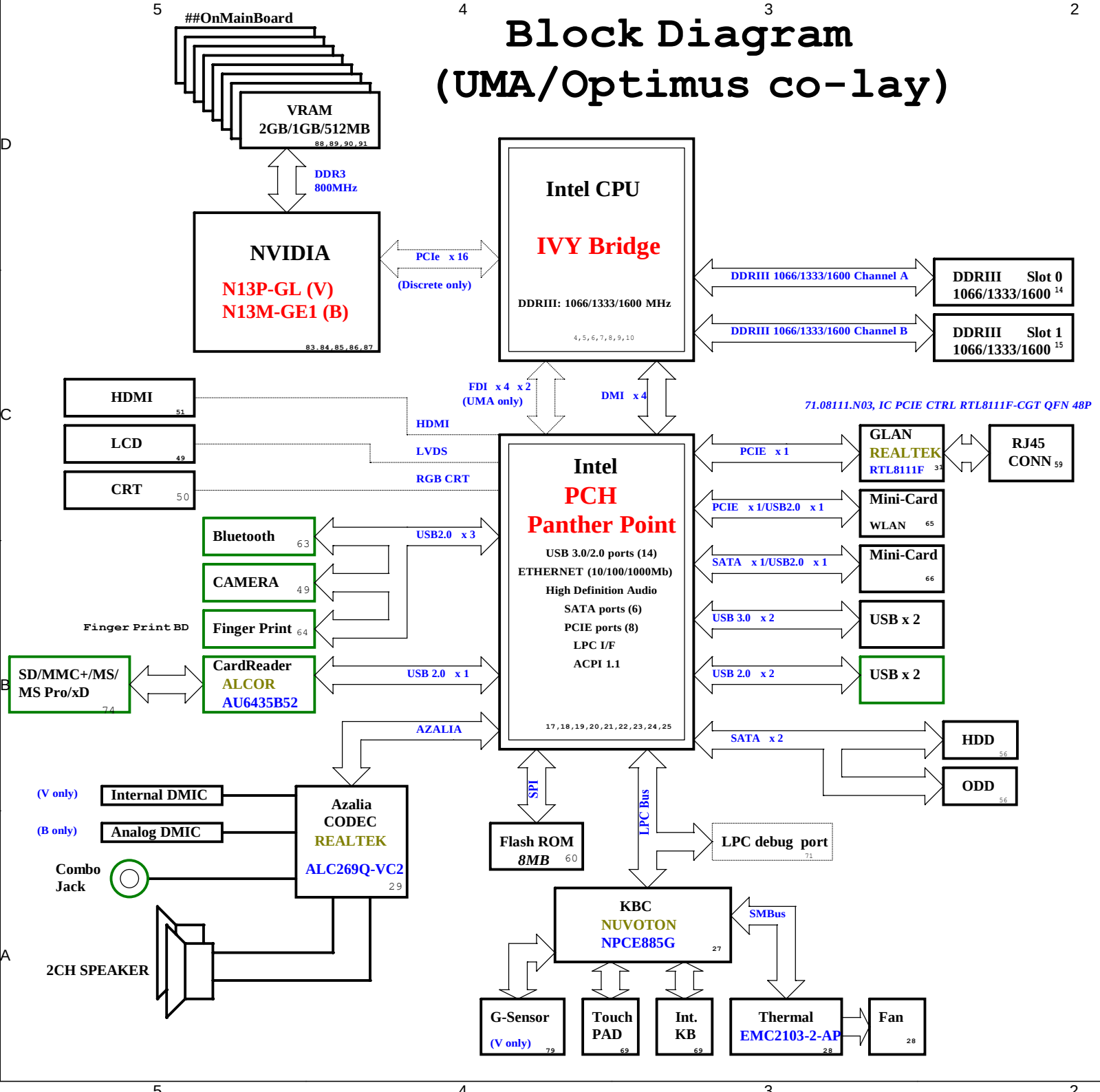
Block Diagram (UMA/Optimus co-lay)



CPU DC/DC TPS51640 42~43	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE

SYSTEM DC/DC TPS51219 45	
INPUTS	OUTPUTS
DCBATOUT	1D05V_VTT

SYSTEM DC/DC TPS51225 41	
INPUTS	OUTPUTS
DCBATOUT	3D3V_AUX_S5 5V_S5 3D3V_S5

SYSTEM DC/DC RT8207M 46	
INPUTS	OUTPUTS
DCBATOUT	0D75V_S0 1D5V_S3 DDR_VREF_S3

SYSTEM DC/DC TPS51640 44	
INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE

VGA TPS51728 92	
INPUTS	OUTPUTS
DCBATOUT	VGA_CORE

TI CHARGER BQ24737 40	
INPUTS	OUTPUTS
+DC_IN_S5 +PBATT	DCBATOUT

SYSTEM DC/DC RT8068A 47	
INPUTS	OUTPUTS
3D3V_S5	1D8V_S0

LDO RT8207 46	
INPUTS	OUTPUTS
5V_S5	0D75V_S0

PCB LAYER

L1:Top	L5:VCC
L2:GND	L6:Signal
L3:Signal	L7:GND
L4:Signal	L8:Signal

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C

Title: Block Diagram

Size	Document Number	Rev
A3	LA480	SD

Date: Friday, January 06, 2012 Sheet 2 of 103

PCH Strapping

Chief River Schematic Checklist Rev0.72

Name	Schematics Notes
SPKR	**Reboot option at power-up** **Default Mode:** Internal weak Pull-down. **No Reboot Mode with TCO Disabled:** Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-up. Leave as "No Connect".
GNT3#/GPIO55 GNT2#/GPIO53 GNT1#/GPIO51	GNT[3:0]# functionality is not available on Mobile. Mobile: Used as GPIO only Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3power rail.
SPI_MOSI	**Enable Danbury:** Connect to Vcc3_3 with 8.2-k? weak pull-up resistor. **Disable Danbury:** Left floating, no pull-down required.
NV_ALE	**Enable Danbury:** Connect to +NVRAM_VCCQ with 8.2-kohm weak pull-up resistor [CRB has it pulled up with 1-kohm no-stuff resistor] **Disable Danbury:** Leave floating (internal pull-down)
NC_CLE	DMI termination voltage. Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	Low (0) - Flash Descriptor Security will be overridden. Also, when this signals is sampled on the rising edge of PWROK then it will also disable Intel ME and its features. High (1) - Security measure defined in the Flash Descriptor will be enabled. Platform design should provide appropriate pull-up or pull-down depending on the desired settings. If a jumper option is used to tie this signal to GND as required by the functional strap, the signal should be pulled low through a weak pull-down in order to avoid asserting HDA_DOCK_EN# inadvertently. Note: CRB recommends 1-kohm pull-down for FD Override. There is an internal pull-up of 20 kohm for DA_DOCK_EN# which is only enabled at boot/reset for strapping functions.
HDA_SDO	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
HDA_SYNC	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
GPIO15	Low (0) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality. High (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality. Note : This is an un-muxed signal. This signal has a weak internal pull-down of 20 kohm which is enabled when PWROK is low. Sampled at rising edge of RSMRST#. CRB has a 1-kohm pull-up on this signal to +3.3VA rail.
GPIO8	GPIO8 on PCH is the Integrated Clock Enable strap and is required to be pulled-down using a 1k +/- 5% resistor. When this signal is sampled high at the rising edge of RSMRST#, Integrated Clocking is enabled, When sampled low, Buffer Through Mode is enabled.
GPIO27	**Default = Do not connect (floating)** High (1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

Processor Strapping

Chief River Schematic Checklist Rev0.72

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[2]	**PCI-Express Static Lane Reversal**	**1:** Normal Operation. **0:** Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	**1**
CFG[4]		**1:** Disabled - No Physical Display Port attached to Embedded DisplayPort. **0:** Enabled - An external Display Port device is connectd to the EMBEDDED display Port	**0**
CFG[6:5]	**PCI-Express Port Bifurcation Straps**	11 : x16 - Device 1 functions 1 and 2 disabled 10 : x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01 : Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00 : x8, x4, x4 - Device 1 functions 1 and 2 enabled	**11**
CFG[7]	**PEG DEFER TRAINING**	**1:** PEG Train immediately following xxRESETB de assertion **0:** PEG Wait for BIOS for training	**1**

POWER PLANE	VOLTAGE	Voltage Rails ACTIVE IN	DESCRIPTION
5V_S0 3D3V_S0 1D8V_S0 1D5V_S0 1D05V_VTT 1D0V_S0 VCCSA 0D75V_S0 VCC_CORE VCC_GFXCORE 1D8V_VGA_S0 3D3V_VGA_S0 1V_VGA_S0	5V 3.3V 1.8V 1.5V 1.05V 1.0V 0.9 - 0.675V 0.75V 0.35V to 1.5V 0.4 to 1.25V 1.8V 3.3V 1V	S0	CPU Core Rail Graphics Core Rail
5V_USBX_S3 1D5V_S3 DDR_VREF_S3	5V 1.5V 0.75V	S3	
BT+ DCBATOUT 5V_S5 5V_AUX_S5 3D3V_S5 3D3V_AUX_S5	6V-14.1V 6V-14.1V 5V 5V 3.3V 3.3V	All S states	AC Brick Mode only
1D05V_LAN	1.05V	S0/M0, SX/M3	ON whenever iAMT is active
3D3V_M 1D05V_M	3.3V 1.05V	S0/M0, SX/M3, WOL_EN	ON for iAMTLegacy WOL
3D3V_AUX_KBC	3.3V	DSW, Sx	ON for supporting Deep Sleep states
3D3V_AUX_S5	3.3V	G3, Sx	Powered by Li Coin Cell in G3 and 3D3V_S5 in Sx

PCIe Routing

LANE1	X
LANE2	Mini Card2 (WWAN)
LANE3	Card Reader
LANE4	Mini Card1 (WLAN)
LANE5	X
LANE6	Intel GBE LAN / LAN
LANE7	X
LANE8	Express Card

USB Table

port9 is debug port

Pair	Device
0	USB3.0 ext port 1
1	USB3.0 ext port 2
2	USB3.0 ext port 3
3	USB3.0 ext port 4
4	BLUETOOTH (USB1.1)
5	Fingerprint (USB1.1)
6	X
7	X
8	Mini Card2 (WWAN)
9	USB ext. port 4 / E-SATA /USB CHARGER
10	CARD READER
11	Mini Card1 (WLAN)
12	CCD
13	New Card

SMBus ADDRESSES

I²C / SMBus Addresses Device	Ref Des	Chief River CRV Address	Hex	Bus
EC SMBus 1 Battery CHARGER				BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA
EC SMBus 2 PCH eDP				SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA
PCH SMBus SO-DIMMA (SPD) SO-DIMMB (SPD) Digital Pot G-Sensor MINI				PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK

SATA Table

SATA Pair	Device
0	HDD1
1	mSATA
2	N/A
3	N/A
4	ODD
5	ESATA

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Title: Table of Content

Size	Document Number	Rev
A3	LA480	SD

Date: Friday, January 06, 2012 Sheet 3 of 103

SSID = CPU

01.00IVY.000 IVY BRIDGE ORCAD SYMBOL.

Note:
Intel DMI supports both Lane Reversal and polarity inversion but only at PCH side. This is enabled via a soft strap.

Signal Routing Guideline:
PEG_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
PEG_ICOMPI & PEG_RCOMPO keep W/S=4/15 mils and routing length less than 500 mils.

Note:
Intel FDI supports both Lane Reversal and polarity inversion but only at PCH side. This is enabled via a soft strap.

Note:
Lane reversal does not apply to FDI sideband signals.

NOTE.
If PEG is not implemented, the RX&TX pairs can be left as No Connect

PEG Static Lane Reversal

NOTE:
Select a Fast FET similar to 2N7002E whose rise/ fall time is less than 6 ns. If HPD on eDP interface is disabled, connect it to CPU VCCIO via a 10-kΩ pull-Up resistor on the motherboard.

Signal Routing Guideline:
EDP_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
EDP_COMPIO keep W/S=4/15 mils and routing length less than 500 mils.

NOTE.
Processor strap CFG[4] should be pulled low to enable Embedded DisplayPort.

SANDY
62.10055.421
2nd = 62.10040.771
SKT-BGA989C470395-1H180

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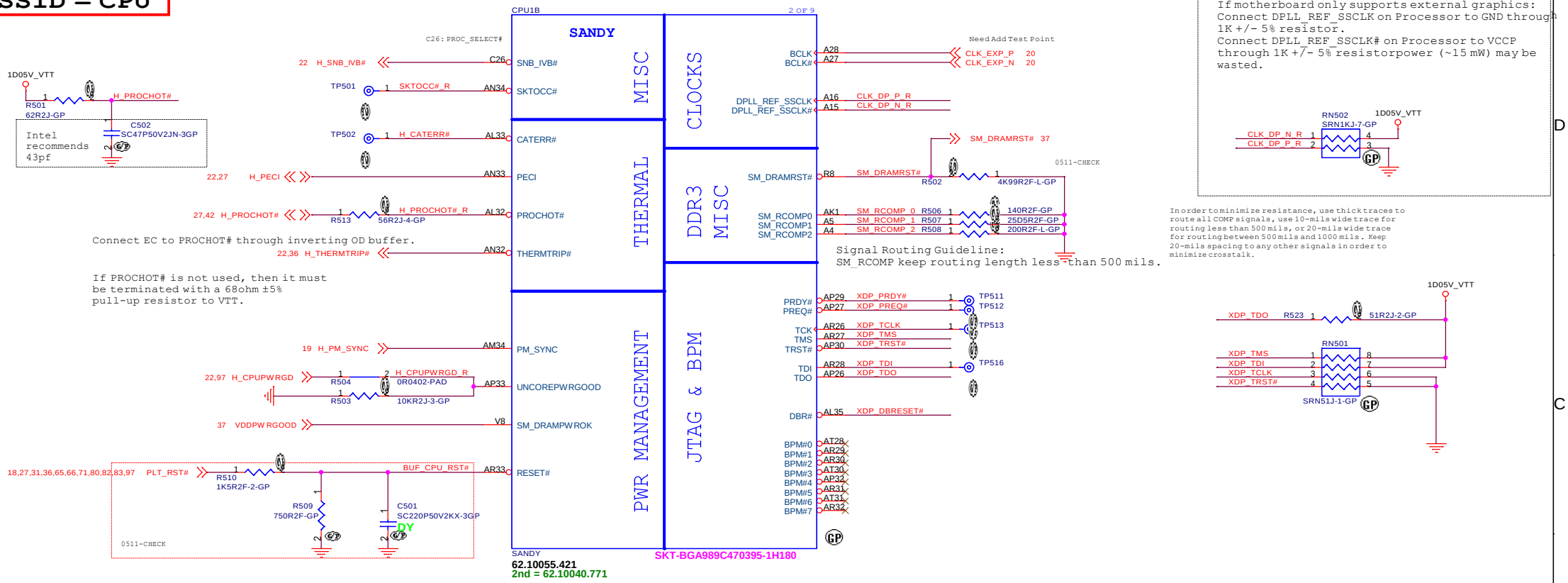
Title: CPU (PCIE/DMI/FDI)
Size: A3 | Document Number: LA480 | Rev: SD
Date: Friday, January 06, 2012 | Sheet 4 of 103

SSID = CPU



Disabling Guidelines:
If motherboard only supports external graphics:
Connect DPLL_REF_SSCLK on Processor to GND through 1K +/- 5% resistor.
Connect DPLL_REF_SSCLK# on Processor to VCCP through 1K +/- 5% resistorpower (~15 mW) may be wasted.

In order to minimize resistance, use thick traces to route all COMP signals, use 10-mils wide trace for routing less than 500 mils, or 20-mils wide trace for routing between 500 mils and 1000 mils. Keep 20-mils spacing to any other signals in order to minimize crosstalk.

DEL U501
DEL R519
DEL C503
DEL R517
DEL R515

ASM R510
ASM R509

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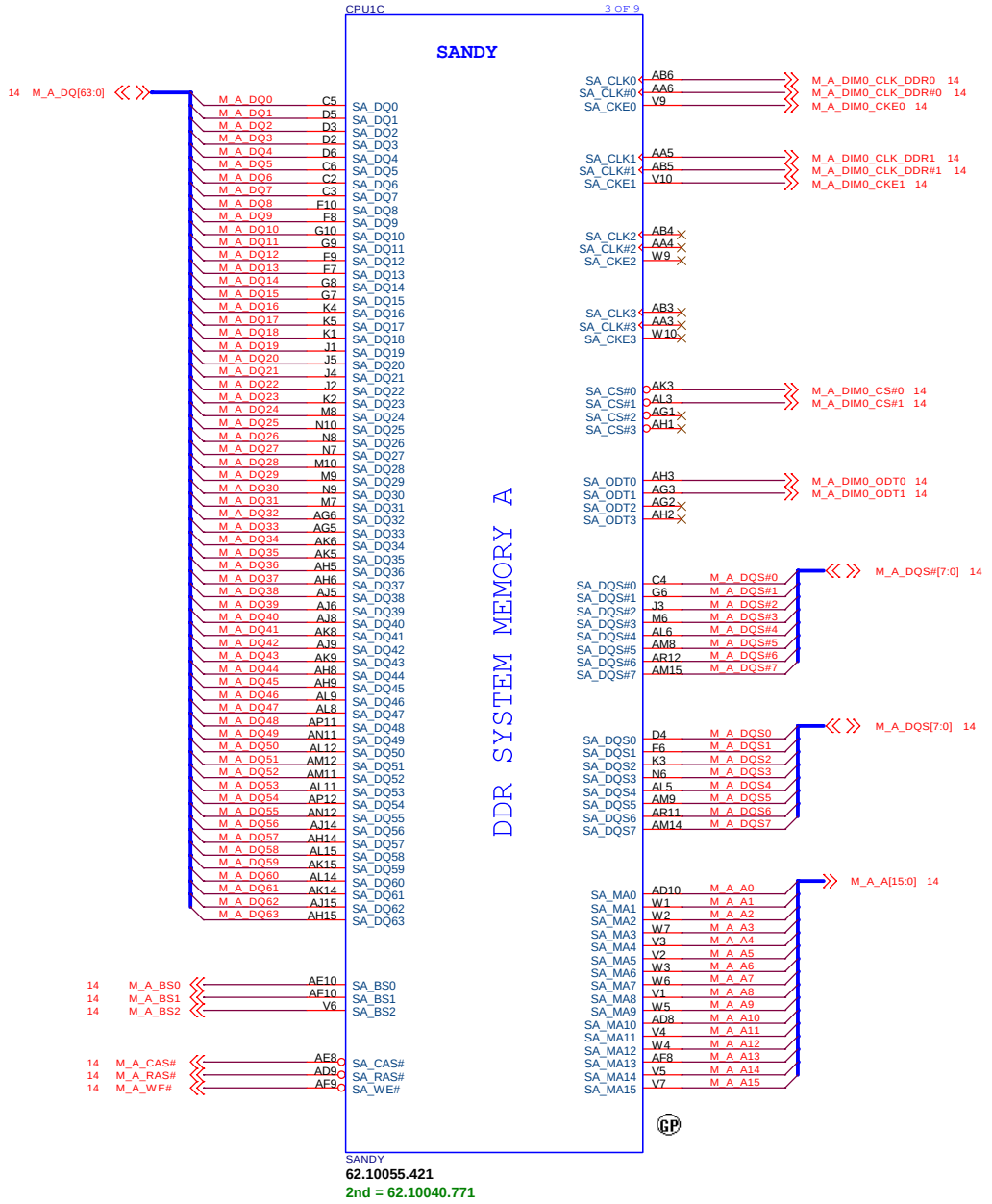
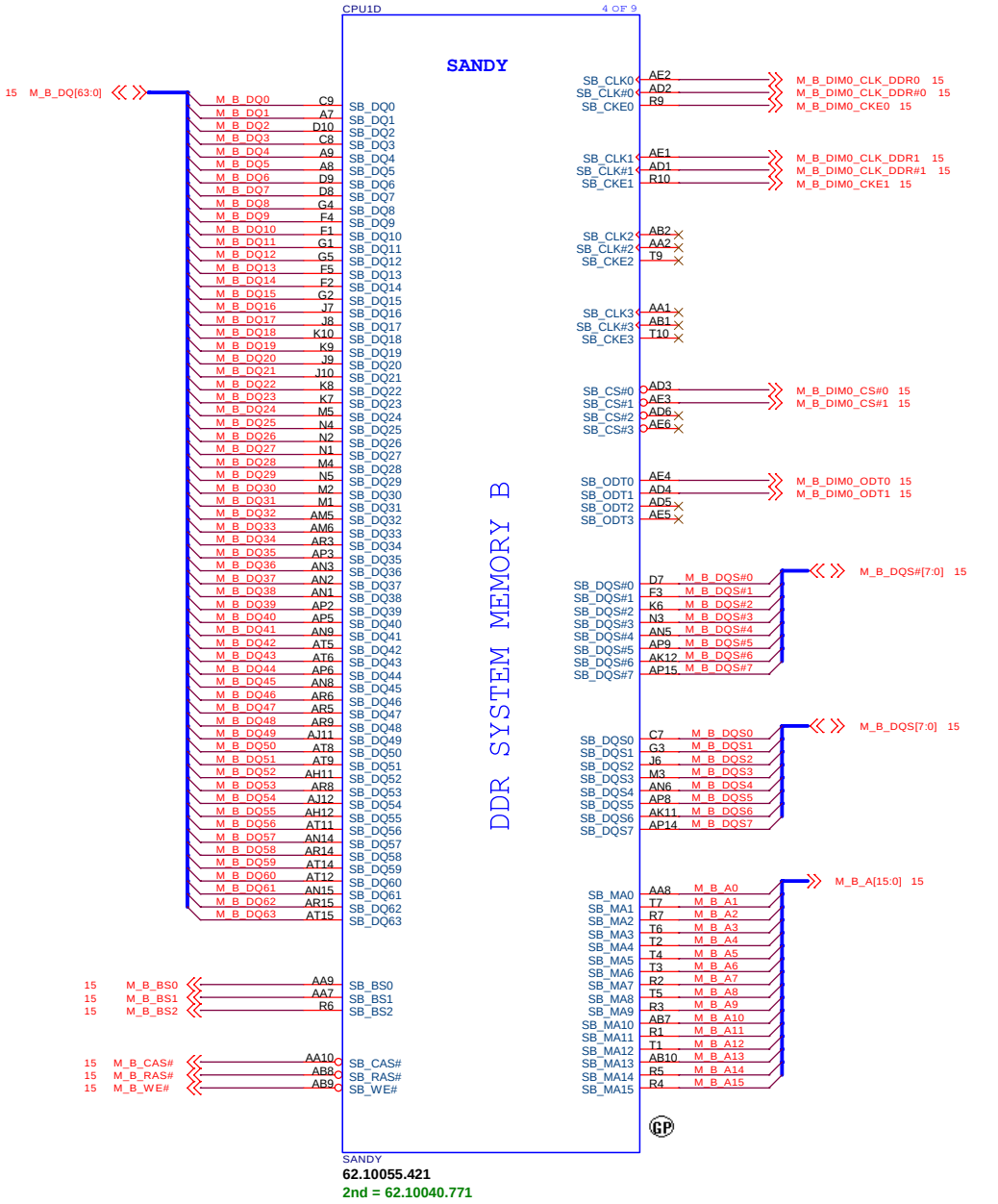
Title: CPU (THERMAL/CLOCK/PM)

Size	Document Number	Rev
A3	LA480	SD

Date: Friday, January 06, 2012 Sheet 5 of 103

SSID = CPU





<Core Design>

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Title: CPU (DDR)

Size: A3 | Document Number: LA480 | Rev: SD

Date: Friday, January 06, 2012 | Sheet 6 of 103

SSID = CPU

CFG2 — R702 1KR2J-1-GP — OPS

PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition 0:Lane Reversed

CFG4 — R703 1KR2J-1-GP — DY

Display Port Presence Strap	
CFG4	1: Disabled; No Physical Display Port attached to Embedded Display Port 0: Enabled; An external Display Port device is connected to the Embedded Display Port

CFG5 — R701 1KR2J-1-GP — DY
CFG6 — R704 1KR2J-1-GP — DY

PCIE Port Bifurcation Straps	
CFG[6:5]	11: x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

CFG7 — R705 1KR2J-1-GP — DY

PEG DEFER TRAINING	
CFG7	1: PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

CPU1E — 5 OF 9 — SANDY

TP717 1 CFG0 — AK28 CFG0
TP702 1 CFG1 — AK29 CFG1
CFG2 — AL26 CFG2
TP703 1 CFG3 — AL27 CFG3
CFG4 — AK26 CFG4
CFG5 — AL29 CFG5
CFG6 — AL30 CFG6
CFG7 — AM31 CFG7
AM32 CFG8
AM30 CFG9
AM28 CFG10
AM26 CFG11
AN28 CFG12
AN31 CFG13
AN26 CFG14
AM27 CFG15
TP704 1 CFG16 — AK31 CFG16
AN29 CFG17

AJ31 RSVD#AJ31
AH31 RSVD#AH31
AJ33 RSVD#AJ33
AH33 RSVD#AH33

AJ26 RSVD#AJ26

12 DDR_W R_VREF01 — B4 RSVD#B4
12 DDR_W R_VREF02 — D1 RSVD#D1

F25 RSVD#F25
F24 RSVD#F24
F23 RSVD#F23
D24 RSVD#D24
G25 RSVD#G25
G24 RSVD#G24
F23 RSVD#E23
D23 RSVD#D23
C30 RSVD#C30
A31 RSVD#A31
B30 RSVD#B30
B29 RSVD#B29
D30 RSVD#D30
B31 RSVD#B31
A30 RSVD#A30
C29 RSVD#C29

J20 RSVD#J20
B18 RSVD#B18
TP705 1 H_VCCP_SEL — A19 RSVD#A19

J15 RSVD#J15

RESERVED

RSVD#L7 L7
RSVD#AG7 AG7
RSVD#AE7 AE7
RSVD#AK2 AK2
RSVD#W8 W8

RSVD#AT26 AT26
RSVD#AM33 AM33
RSVD#AJ27 AJ27

RSVD#T8 T8
RSVD#J16 J16
RSVD#H16 H16
RSVD#G16 G16

RSVD#AR35 AR35
RSVD#AT34 AT34
RSVD#AT33 AT33
RSVD#AP35 AP35
RSVD#AR34 AR34

RSVD#B34 B34
RSVD#A33 A33
RSVD#A34 A34
RSVD#B35 B35
RSVD#C35 C35

RSVD#AJ32 AJ32
RSVD#AK32 AK32

RSVD#AH27 AH27 TP713 1 TP720

RSVD#AN35 AN35 CLK_XDP_ITP_P 1 TP718
RSVD#AM35 AM35 CLK_XDP_ITP_N 1 TP719

RSVD#AT2 AT2
RSVD#AT1 AT1
RSVD#AR1 AR1

SANDY SKT-BGA989C470395-1H180
62.10055.421
2nd = 62.10040.771

<Core Design>

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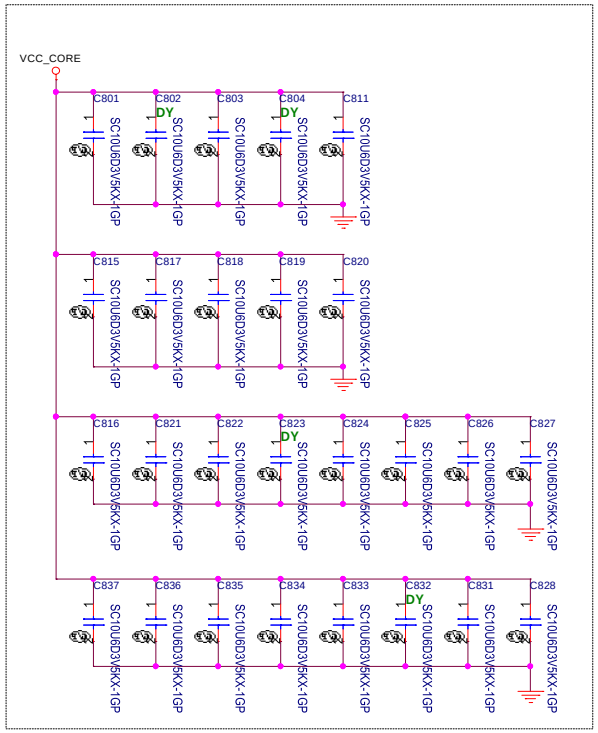
Title: CPU (RESERVED)
Size: A3 | Document Number: LA480 | Rev: SD
Date: Friday, January 06, 2012 | Sheet 7 of 103

POWER

VCC CORE : 53A

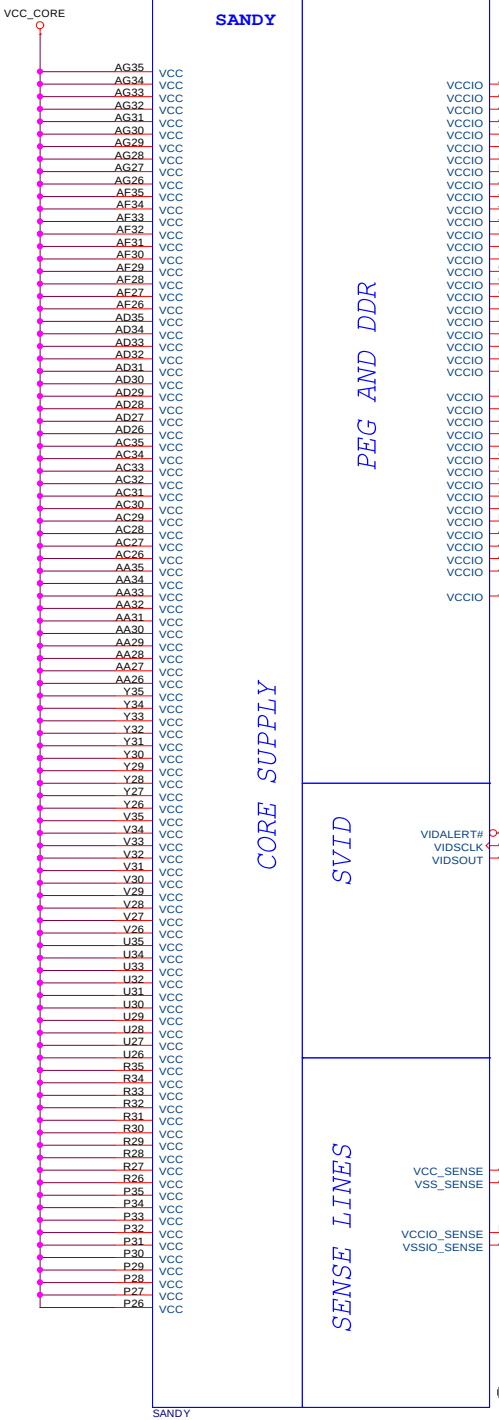
0511-CHECKCAP.



CPU1F

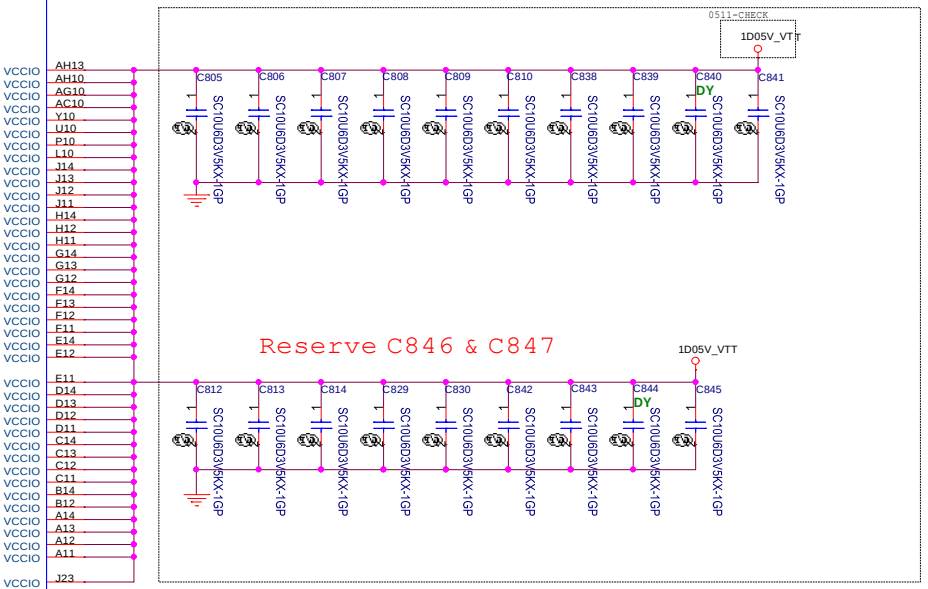
6 OF 9

SANDY

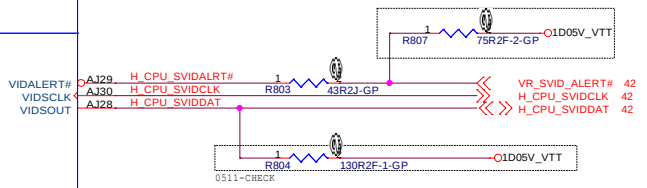


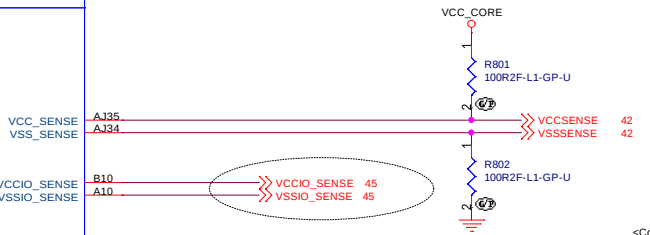
VCCIO : 8.5A

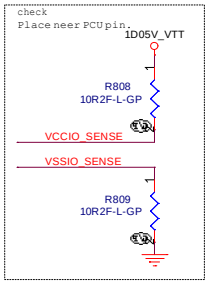
0511-CHECKCAP.



For CRB VIDSOUT need to pull high 130 ohm closr to CPU and IMVP7
For CRB VIDALERT# need to pull high 75 ohm close to CPU







SANDY

62.10055.421

2nd = 62.10040.771

<Core Design>

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Title	CPU (VCC CORE)	
Size: Custom	Document Number: LA480	Rev: SD
Date: Friday, January 06, 2012	Sheet 8 of 103	

0511-CHECK CAP

POWER

VCC_GFXCORE

PROCESSOR VAXG: 24A

0511-CHECK

C901 C902 C903 C904 C905 C906 RC901 — SC10U6D3V5KX-1GP / DY SC33P50V2JN-3GP

C907 C908 C918 C919 C920 C921 RC902 — SC10U6D3V5KX-1GP / DY SC33P50V2JN-3GP

CPU1G — 7 OF 9

SANDY

AT24 AT23 AT21 AT20 AT18 AT17 AR24 AR23 AR21 AR20 AR18 AR17 AP24 AP23 AP21 AP20 AP18 AP17 AN24 AN23 AN21 AN20 AN18 AN17 AM24 AM23 AM21 AM20 AM18 AM17 AL24 AL23 AL21 AL20 AL18 AL17 AK24 AK23 AK21 AK20 AK18 AK17 AJ24 AJ23 AJ21 AJ20 AJ18 AJ17 AH24 AH23 AH21 AH20 AH18 AH17 — VAXG

GRAPHICS

SENSE LINES

VAXG_SENSE — AK35
VSSAXG_SENSE — AK34

VCC_AXG_SENSE 42
VSS_AXG_SENSE 42

Refer to the latest Huron River Mainstream PDG (Doc# 436735) for more details on S3 power reduction implementation.

+V SM VREF CNT should have 10 mil trace width

VREF

SM_VREF — AL1

+V_SM_VREF_CNT 37

Routing Guideline:
Power from DDR_VREF_S3 and +V_SM_VREF_CNT should have 10 mils trace width.

DDR3 -1.5V RAILS

VDDQ: 5A

1D5V_S0

VDDQ — AE7 AF4 AF1 AC7 AC4 AC1 Y7 Y4 Y1 U7 U4 U1 P7 P4 P1

C909 DY C910 C911 C912 C913 C914 — SC10U6D3V5KX-1GP

SA RAIL

VCCA: 6A

VCCSA

C916 C915 C917 — SC10U6D3V5KX-1GP

VCCSA — M27 M26 L26 J26 J25 J24 H26 H25

+V0.85S – VCCSA – System Agent rail voltage can be
[0.9, 0.725, 0.8, 0.675] V for IVB
[0.9, 0.8] V for SNB

MISC

VCCSA_SENSE — H23

VCCSA_SENSE 48

FC_C22 — C22
VCCSA_VID1 — C24

VCCSA_SELECT0 48
VCCSA_SELECT1 48

RN901 SRN1KJ-7-GP

1.8V RAIL

1D8V_S0

VCCPLL: 1.2A

C926 C923 C922 C924 — SC10U6D3V5KX-1GP / SC1U10V2KX-1GP

VCCPLL — B6 A6 A2

SANDY
62.10055.421
2nd = 62.10040.771

VCC_GFXCORE

R906 100R2F-L1-GP-U
VCC_AXG_SENSE
VSS_AXG_SENSE
R907 100R2F-L1-GP-U

<Core Design>

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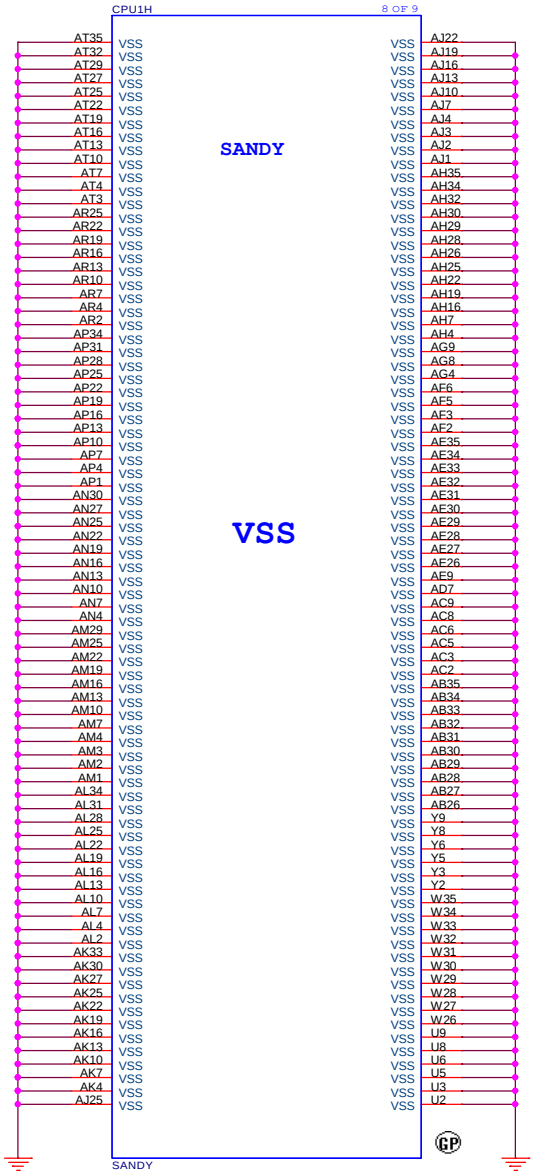
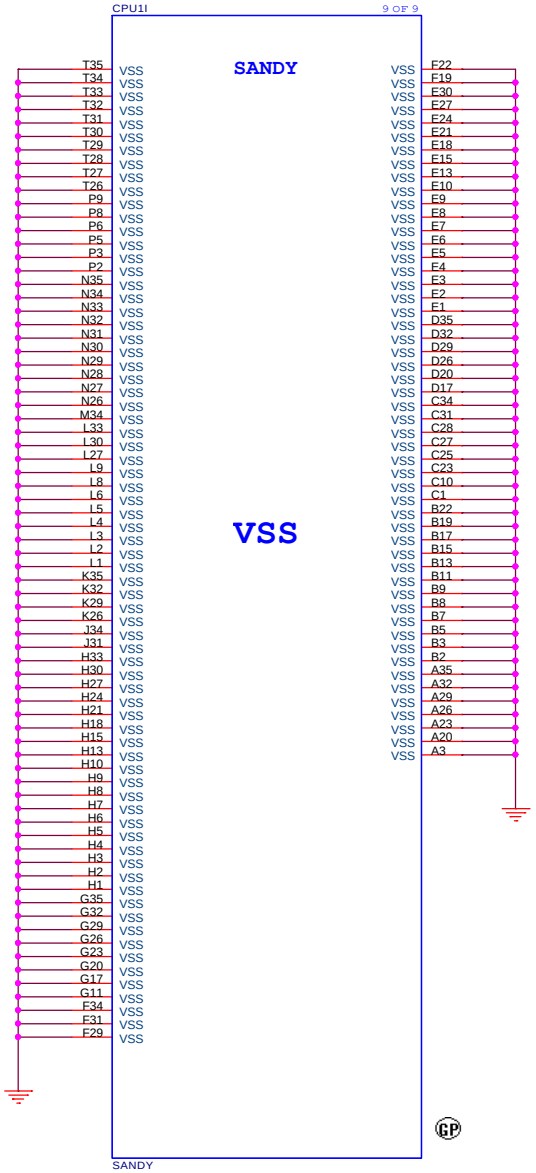
Title: CPU (VCC_GFXCORE)

Size: A3 | Document Number: LA480 | Rev: SD

Date: Friday, January 06, 2012 | Sheet 9 of 103

SSID = CPU





<Core Design>

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Title: *CPU (VSS)*

Size	Document Number	Rev
A3	LA480	SD

Date: Friday, January 06, 2012 Sheet 10 of 103

5 4 3 2 1

D

C

B

A

BLANK

<Core Design>

緯創資通

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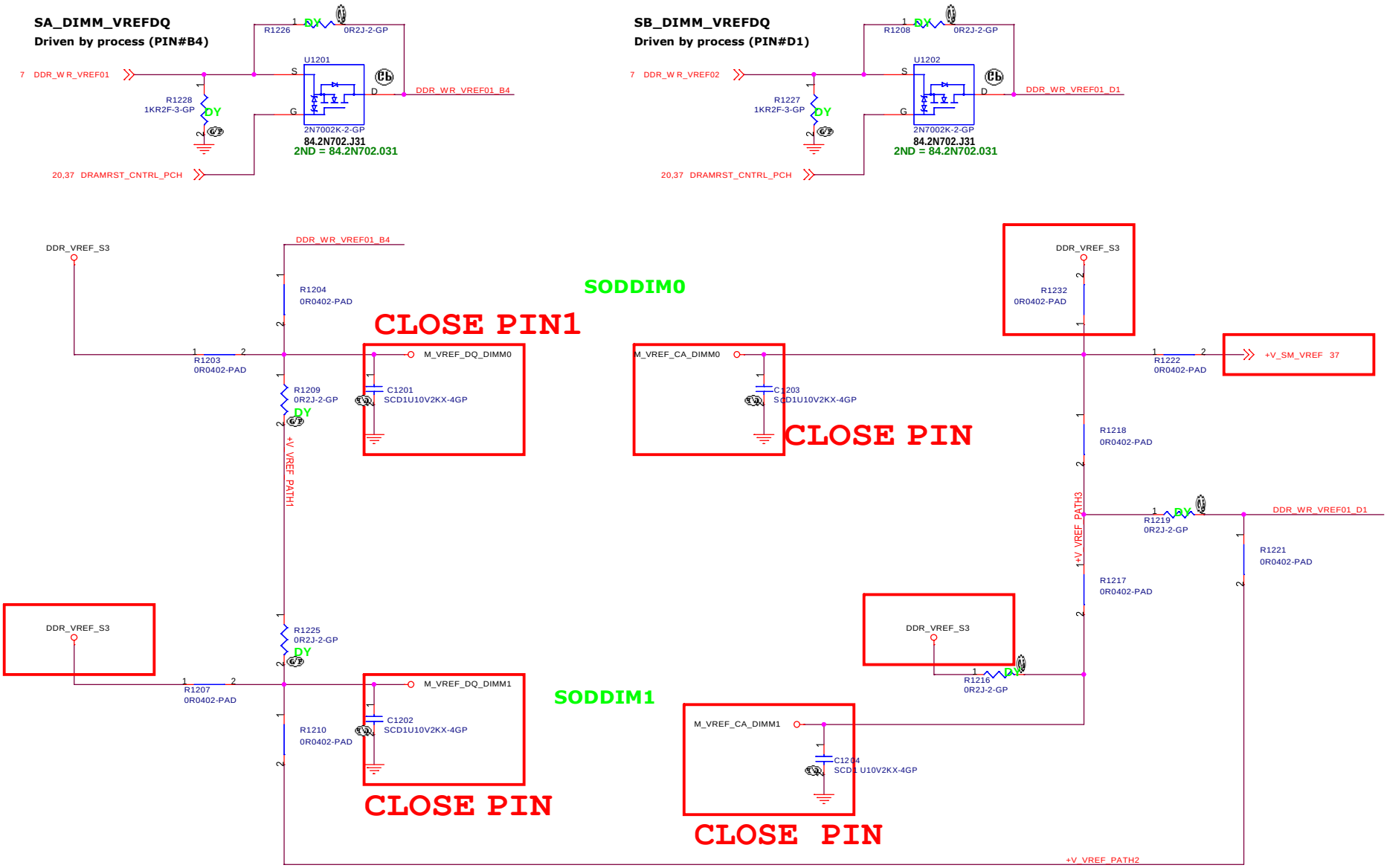
Taipei Hsien 221, Taiwan, R.O.C

Title: <Title>		
Size: A4	Document Number: LA480	Rev: SD
Date: Friday, January 06, 2012	Sheet 11 of 103	

VREF circuit -M1 (Voltage Driver Network) & M3 (Driven by Processor) Implementation

CAD Note: All VREF traces should have 20:20 mil trace geometry. Note that while 20 mil trace width is optimal, short violations is acceptable if required due to tight routing constraints.



<Core Design>

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Title		
M3		
Size: A3	Document Number: LA480	Rev: SD
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5 4 3 2 1

D

C

B

A

BLANK

<Core Design>

緯創資通

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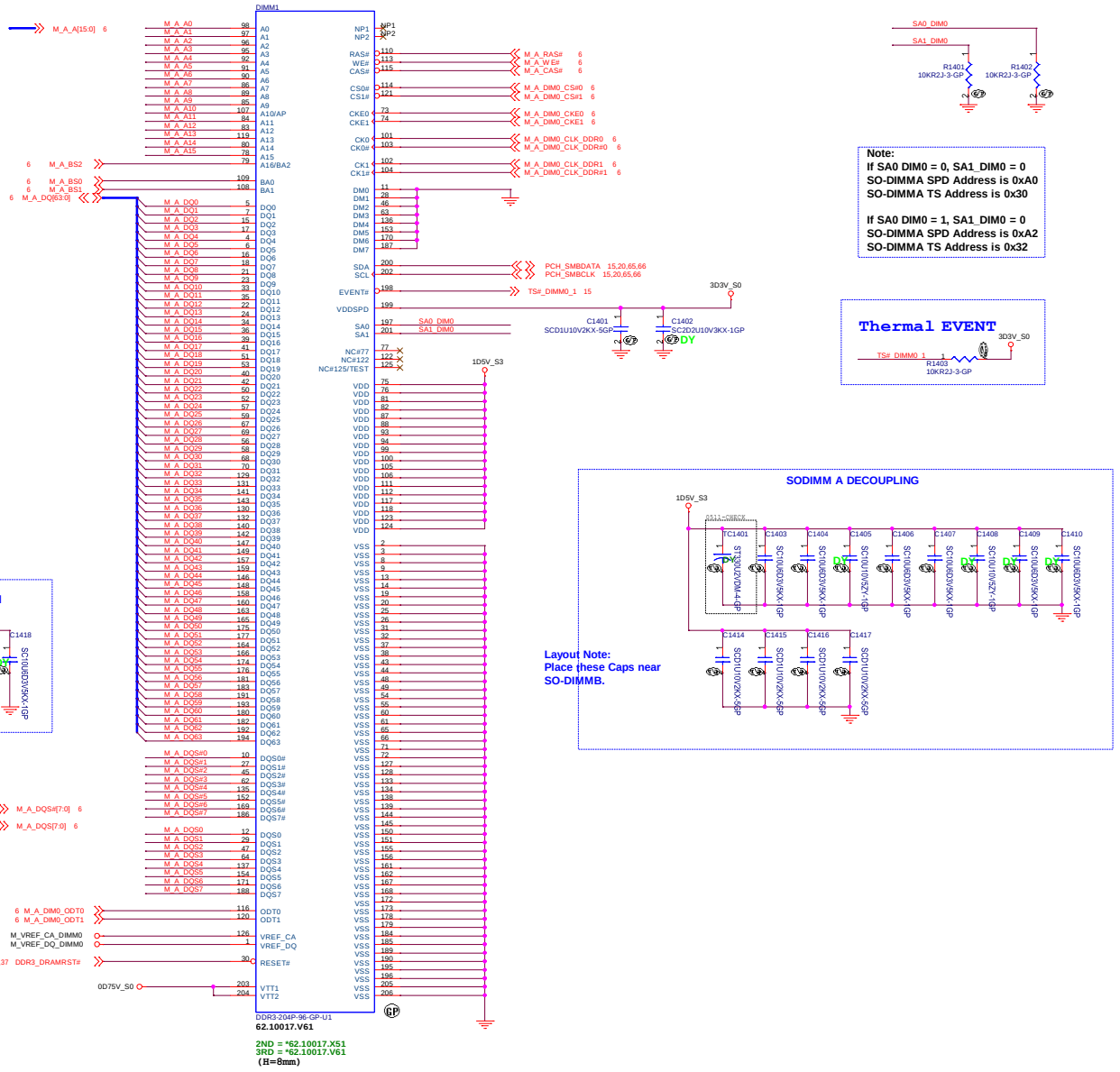
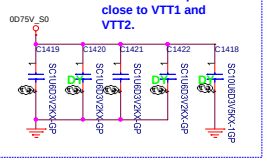
Title: <Title>		
Size: A4	Document Number: LA480	Rev: SD
Date: Friday, January 06, 2012	Sheet 13 of 103	

SSID = MEMORY



Place these caps close to VTT1 and VTT2.



Note:
If SA0 DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30

If SA0 DIM0 = 1, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA2
SO-DIMMA TS Address is 0x32

Thermal EVENT

SODIMM A DECOUPLING

Layout Note:
Place these Caps near SO-DIMMB.

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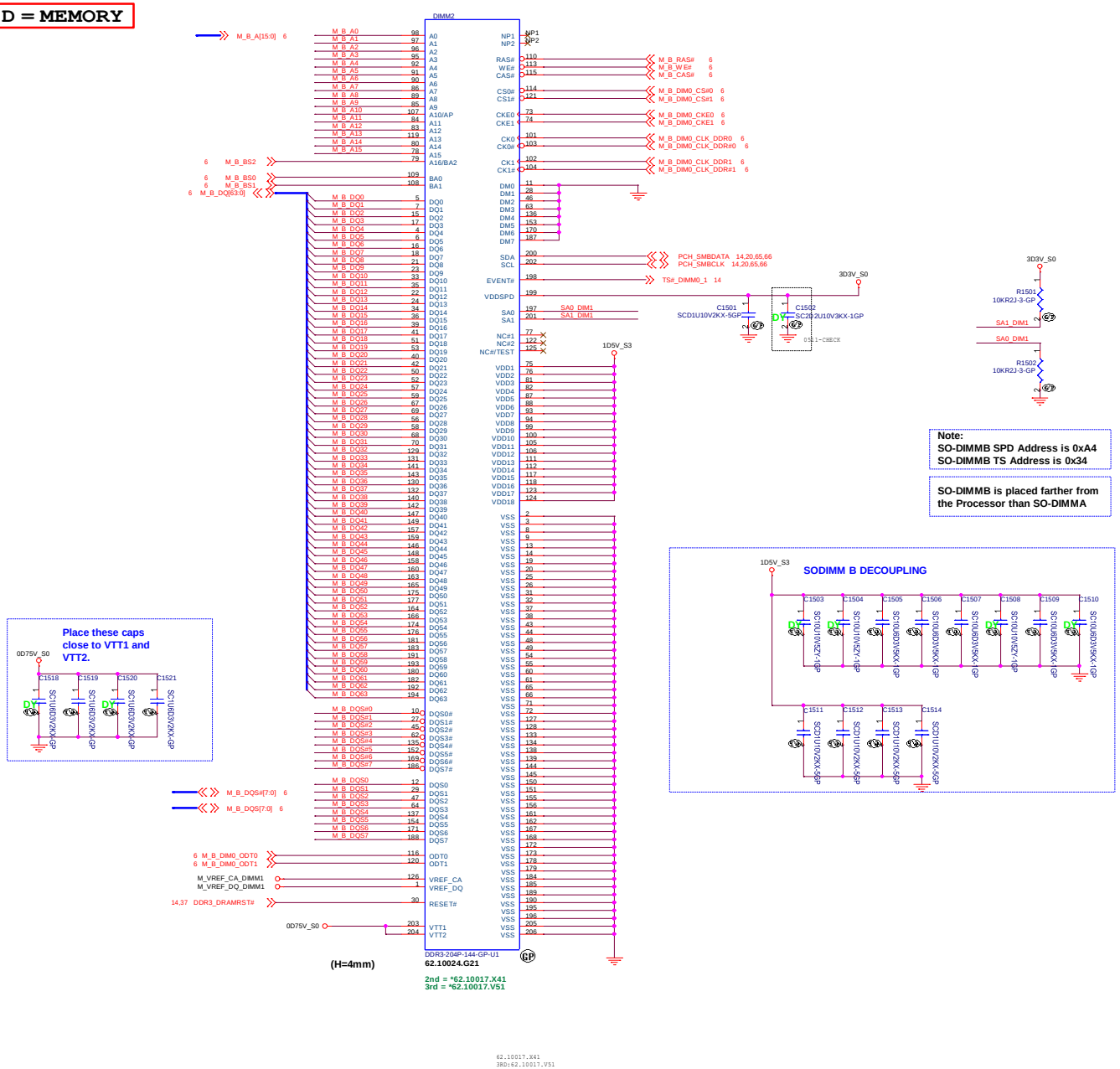
Title: **DDR3-SODIMM1**

Size: A2 | Document Number: **LA480** | Rev: **SD**

Date: Friday, January 06, 2012 | Sheet 14 of 103

SSID = MEMORY



Place these caps close to VTT1 and VTT2.

Note:
SO-DIMMB SPD Address is 0xA4
SO-DIMMB TS Address is 0x34

SO-DIMMB is placed farther from the Processor than SO-DIMMA

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Title: **DDR3-SODIMM2**

Size	Document Number	Rev
A2	LA480	SD

Date: Friday, January 06, 2012 Sheet 15 of 103

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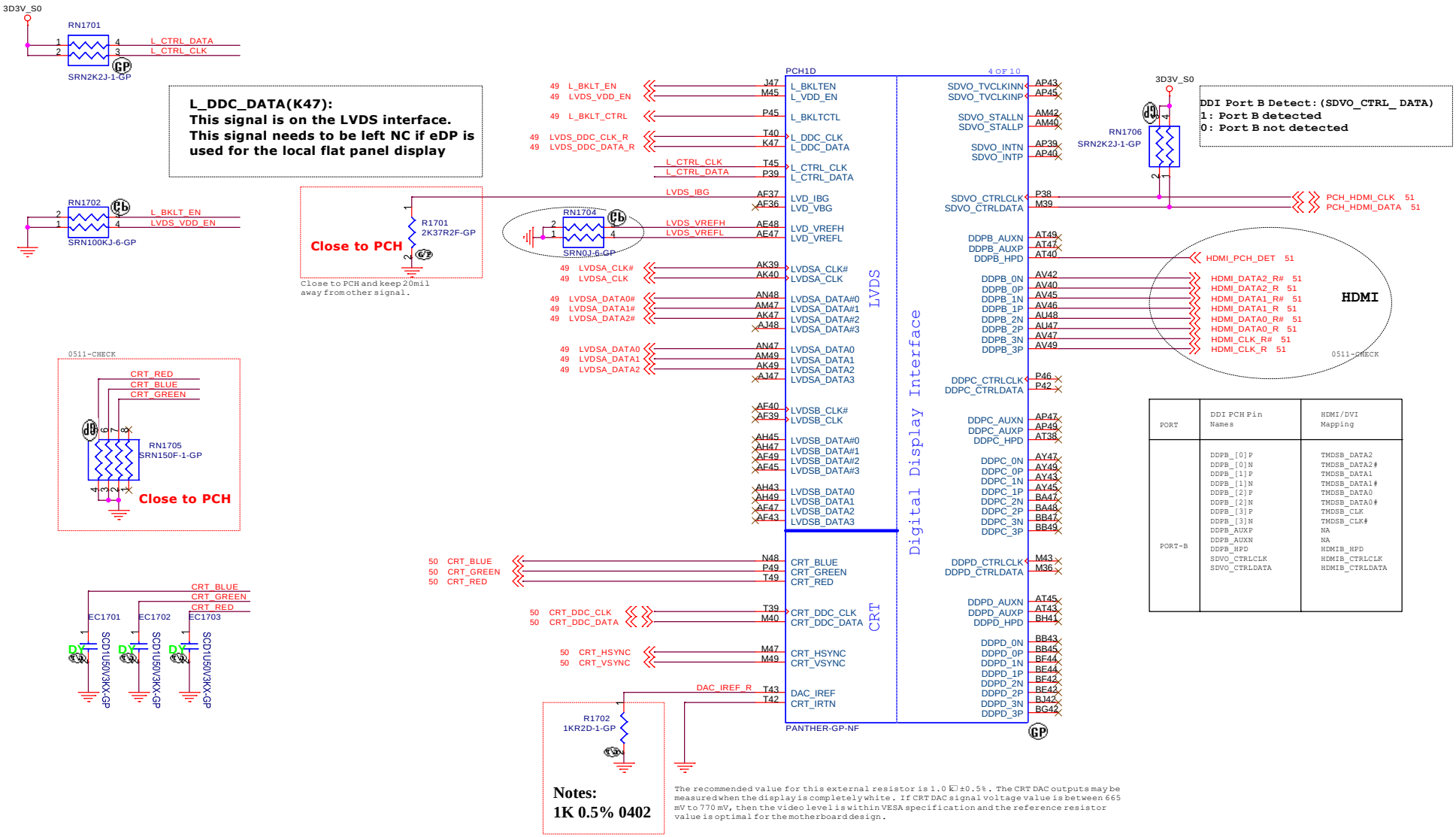
Title: ***DDR3-SODIMM2***

Size	Document Number	Rev
A4	**LA480**	**SD**

Date: Friday, January 06, 2012 Sheet 16 of 103



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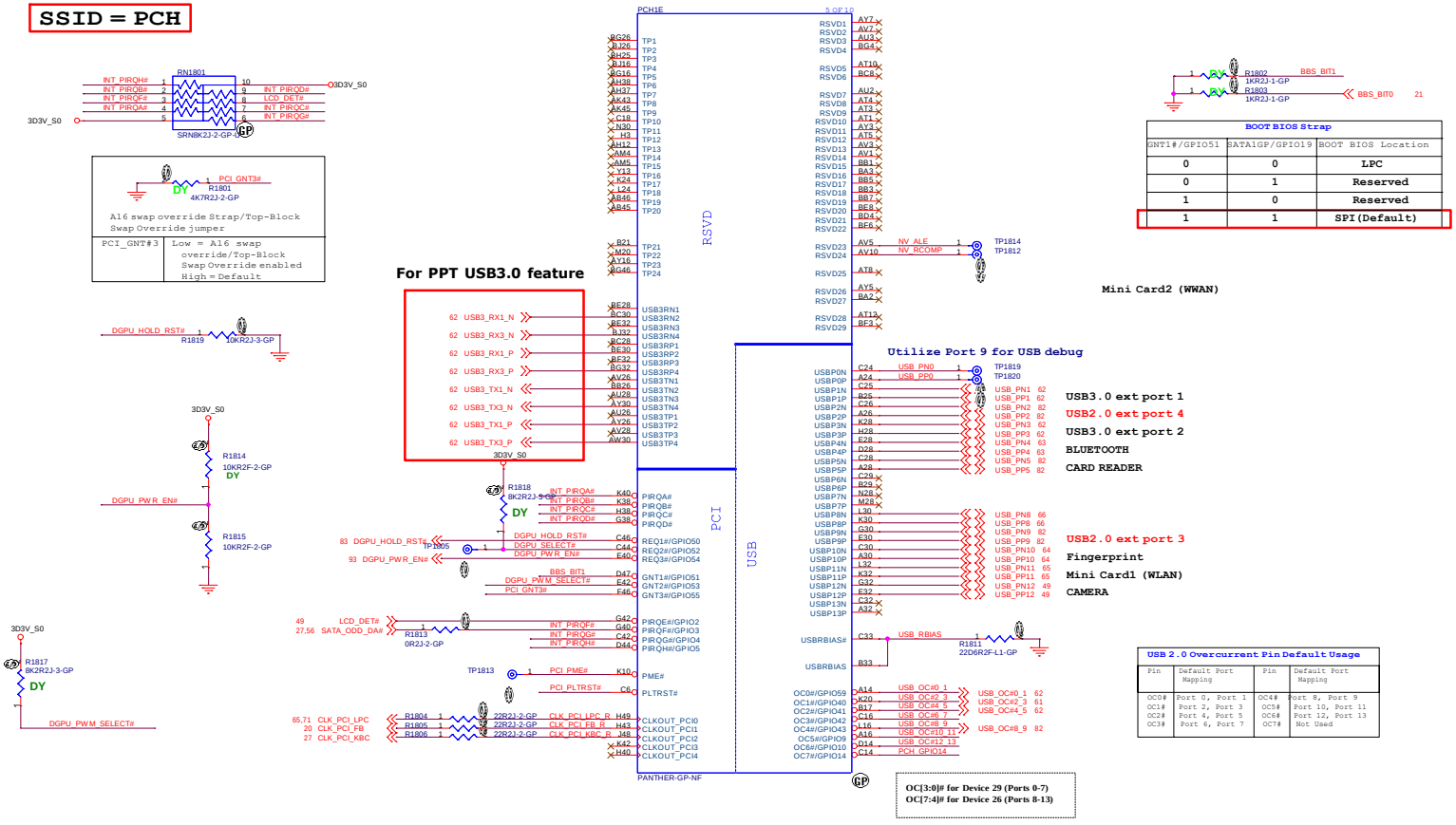
Title: **PCH : LVDS/CRT/DDI**

Size	Document Number	Rev
A3	LA480	SD

Date: Friday, January 06, 2012 Sheet 17 of 103

SSID = PCH



BOOT BIOS Strap		
GNT1#/GPIO51	SATA1GP/GPIO19	BOOT BIOS Location
0	0	LPC
0	1	Reserved
1	0	Reserved
1	1	SPI(Default)

A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default

USB 2.0 Overcurrent Pin Default Usage			
Pin	Default Port Mapping	Pin	Default Port Mapping
OC0#	Port 0, Port 1	OC4#	Port 8, Port 9
OC1#	Port 2, Port 3	OC5#	Port 10, Port 11
OC2#	Port 4, Port 5	OC6#	Port 12, Port 13
OC3#	Port 6, Port 7	OC7#	Not Used

Gx8 USB Table

Pair	Device
0	X
1	USB3.0, ext port1
2	USB2.0, ext port4
3	USB3.0, ext port2
4	Bluetooth
5	CARD READER
6	X
7	X
8	3G
9	USB2.0, ext. port 3
10	Finger Print
11	Mini Card1 (WLAN)
12	CAMERA
13	X

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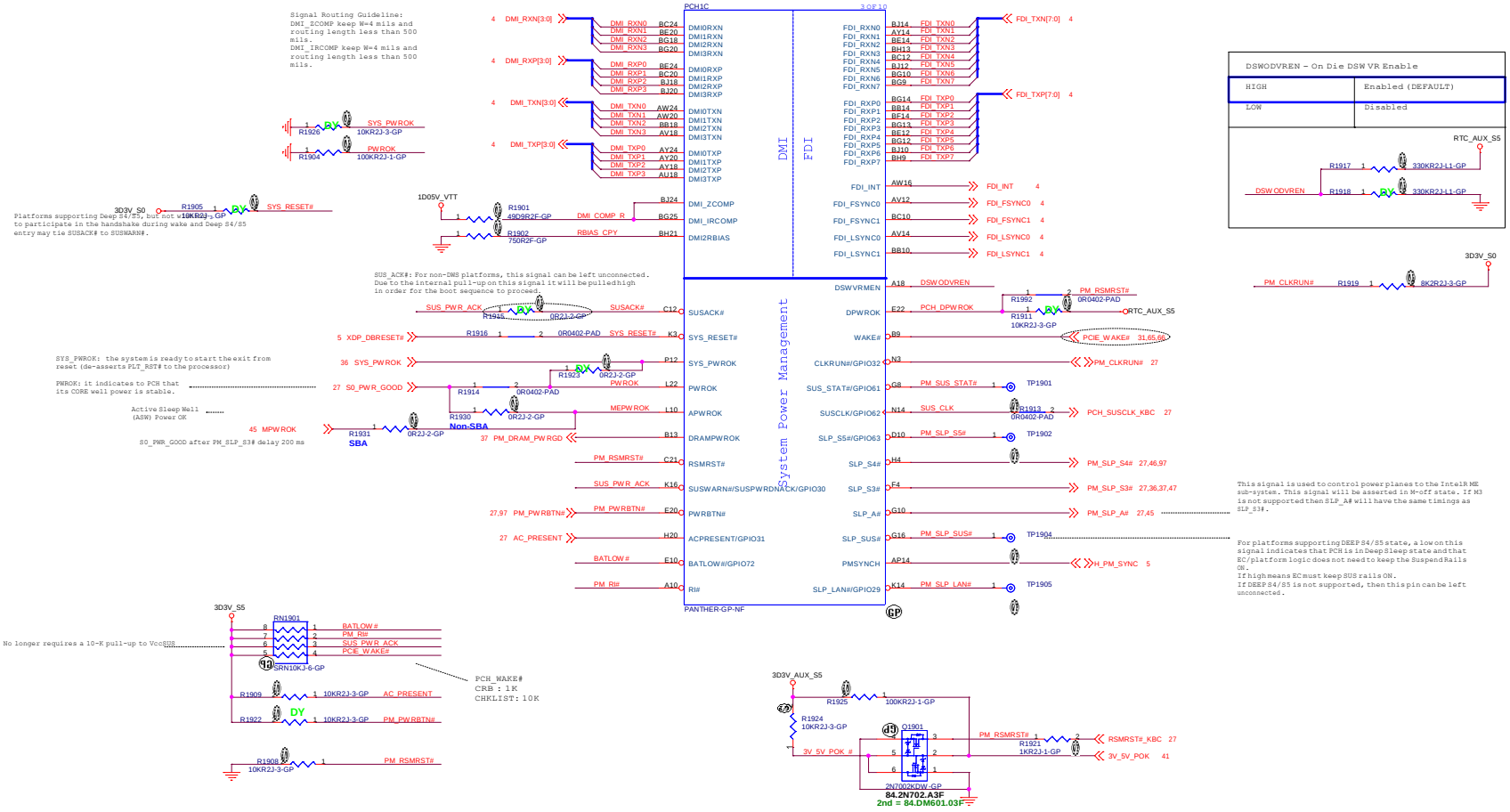
Title: PCH : PCI/USB/NVRAM/RSVD

Size: A2 | Document Number: LA480 | Rev: SD

Date: Friday, January 06, 2012 | Sheet 18 of 103

SSID = PCH

For platforms not supporting Deep S4/S5
1.VccSUS3_3 and VccDSW3_3 will rise at the same time (connected on board)
2.DPWROK and RSMRST# will rise at the same time (connected on board)
3.SLP_SUS# and SUSACK# are left as 'no connect'
4.SUSWARN# used as SUSPWRDNACK/GPIO30



<Core Design>

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Title: PCH : DMI/FDI/PM		
Size: A2	Document Number: LA480	Rev: SD
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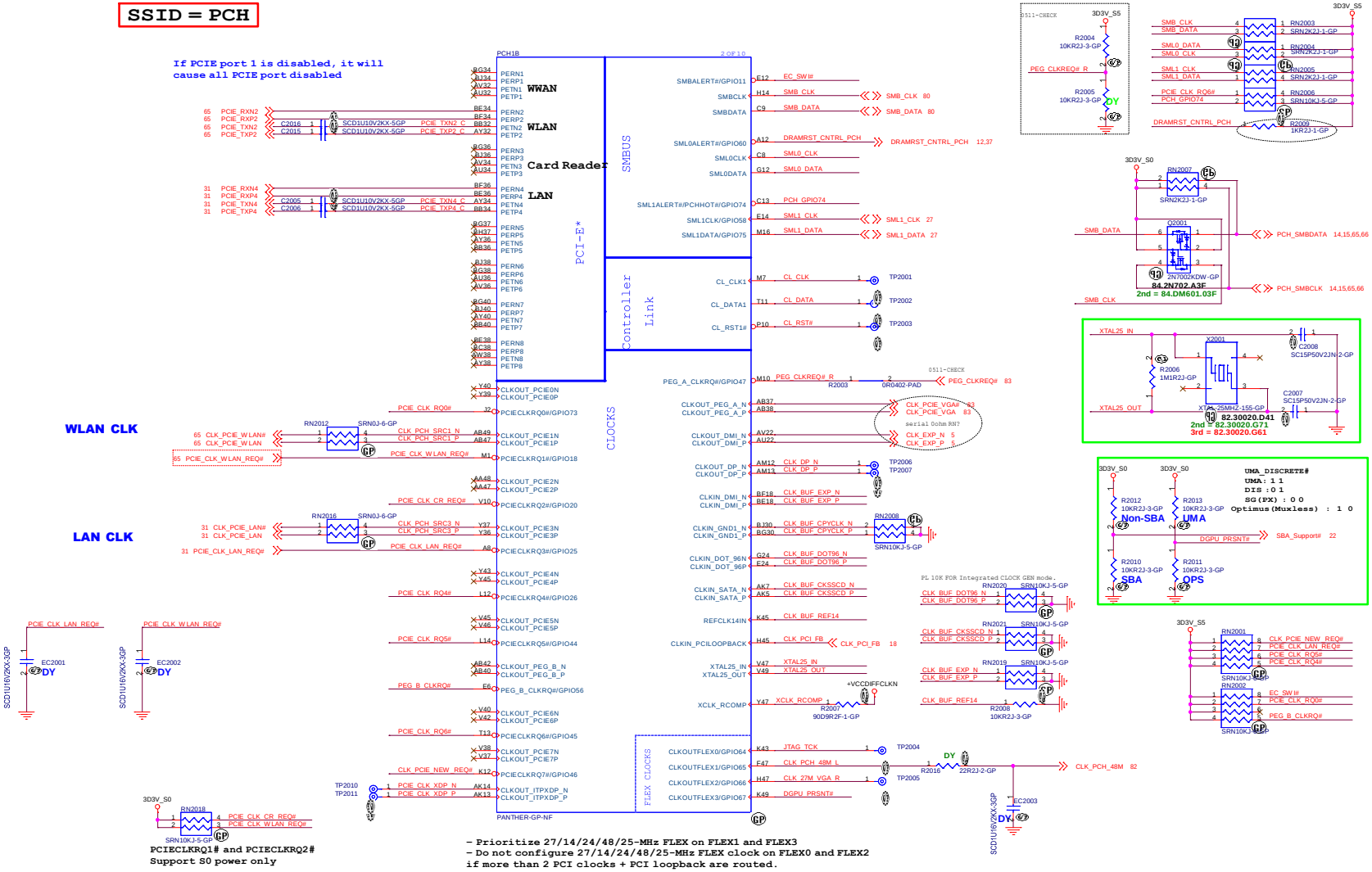
SSID = PCH

If PCIE port 1 is disabled, it will cause all PCIE port disabled



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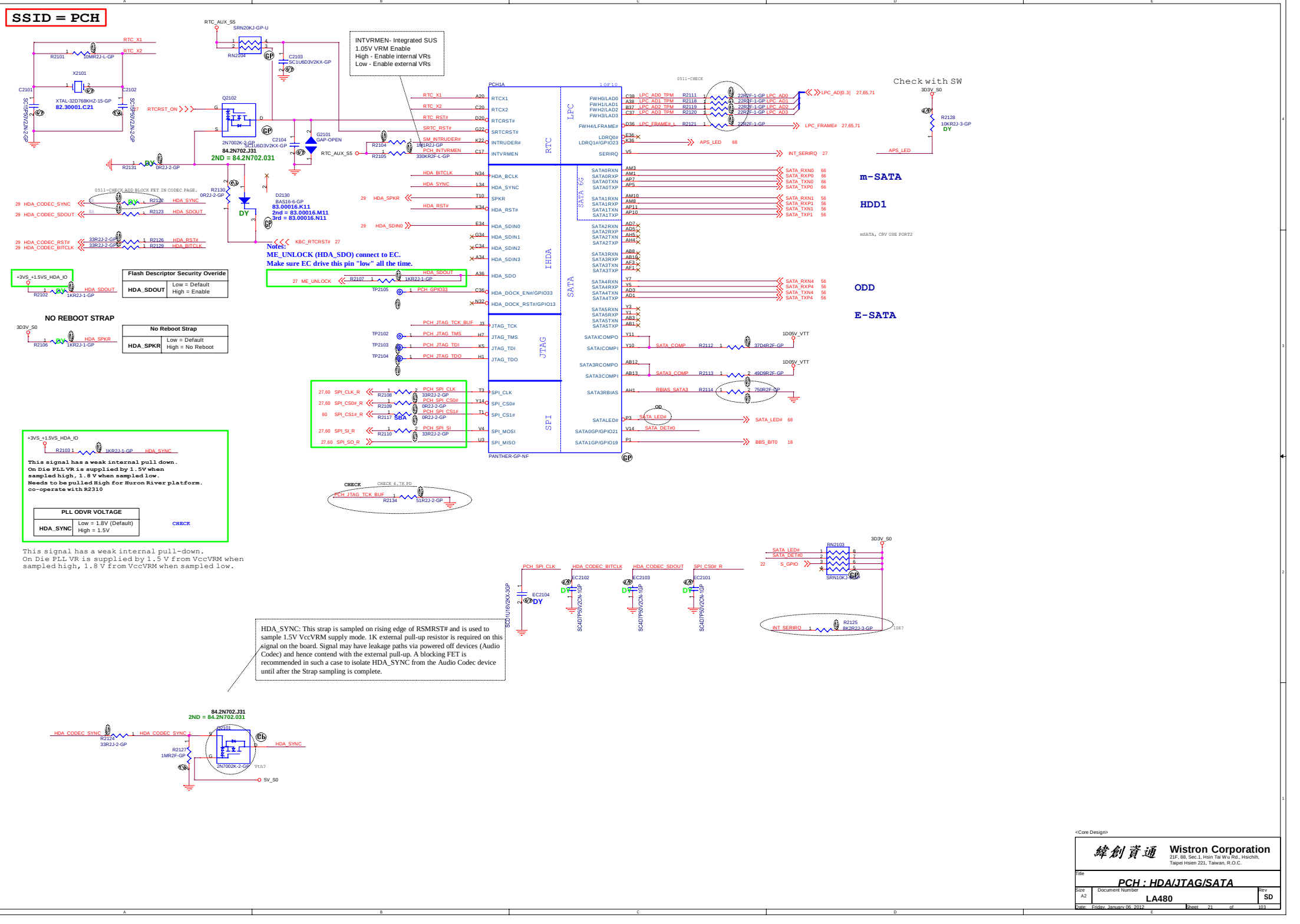
Title: PCH : PCIE/SMBUS/CLK

Size: A2 | Document Number: LA480 | Rev: SD

Date: Friday, January 06, 2012 | Sheet 20 of 103

SSID = PCH



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Title: PCH : HDA/JTAG/SATA

Size	Document Number	Rev
A2	LA480	SD

Date: Friday, January 06, 2012 Sheet 21 of 103

R2202
HR:200K (64.20035.6DL)
CRV:10K (63.10334.1DL)

3D3V_S0 — R2202 1 — 10KR2J-3-GP — SATA_ODD_PRSNT#

3D3V_S0 — RN2203 — H_A20GATE, H_RCIN# — SRN10KJ-5-GP

GPIO27 has a weak [20K] internal pull up. To enable on-die PLL Voltage regurator, should not place external pull down.

G-Sensor	ST	KIXNOK
R2226	DY	10K
R2221	10K	DY

Note:
For PCH debug with XDP, need to NO STUFF R2218

PCH1F — 6 OF 10 — PANTHER-GP-NF

GPIO:
- 21 S_GPIO — R2218 — 10OR2J-2-GP — GPIO0 — T7 — BMBUSY#/GPIO0
- EC_SMI# — A42 — TACH1/GPIO1
- DGPU_HPD_INTR# — H36 — TACH2/GPIO6
- 27 EC_SC# — E38 — TACH3/GPIO7
- ICC_EN# — C10 — GPIO8
- 60 RTC_DET# — C4 — LAN_PHY_PWR_CTRL/GPIO12
- PCH_GPIO15 — G2 — GPIO15
- 56 SATA_ODD_PRSNT# — R2215 — 0R2J-2-GP — PCH_GPIO16 — U2 — SATA4GP/GPIO16
- 92,93 DGPU_PWROK — R2216 — 0R2J-2-GP — DGPU_PWROK_C — D40 — TACH0/GPIO17
- PCH_GPIO22 — T5 — SCLOCK/GPIO22
- Gsensor_ID — E8 — GPIO24
- PCH_GPIO27 — E16 — GPIO27
- PLL_ODVR_EN — P8 — GPIO28
- PSW_CLR# — K1 — STP_PCI#/GPIO34
- FP_DET# — K4 — GPIO35
- DMI_OVRVLTG — V8 — SATA2GP/GPIO36
- FDI_OVRVLTG — M5 — SATA3GP/GPIO37
- MFG_MODE — N2 — SLOAD/GPIO38
- GFX_CRB_DET — M3 — SDATAOUT1/GPIO48
- PCH_GPIO48 — V13 — SDATAOUT1/GPIO48
- PCH_TEMP_ALERT# — V3 — SATA5GP/GPIO49/TEMP_ALERT#
- USB3_PWR_ON — D6 — GPIO57

CPU/MISC:
- SATA_ODD_PWRGT — 56 — C40 — TACH4/GPIO68
- SBA_Support# — 20 — B41 — TACH5/GPIO69
- C41 — VRAM_SIZE1 — TACH6/GPIO70
- A40 — VRAM_SIZE2 — TACH7/GPIO71
- P4 — H_A20GATE — 27 — A20GATE
- AU16 — H_PECI_R — R2203 — 0R2J-2-GP — H_PECI — 5,27 — PECI
- P5 — H_RCIN# — 27 — RCIN#
- AY11 — H_CPUPWRGD — 5,97 — PROCPWRGD
- AY10 — PCH_THERMTRIP_R — R2204 — 39OR2J-1-GP — H_THERMTRIP# — 5,36 — THRMTRIP#
- T14 — INIT3_3V# — TP2201 — INIT3_3V#
- AY1 — NV_CLE — DF_TVS
- AH8, AK11, AH10, AK10 — TS_VSS1..4 — TS_VSS — R2219 — 0R0402-PAD
- P37 — NC_1

PROCPWRGD (PCH) --> UNCOREPOWRGOOD (CPU)
Indicates that VccSA, VDDQ, VccA (1.8V) and VccIO power supplies are stable. This signal will be asserted only after PWROKassertion.

TS Signal Disable Guideline:
TS_VSS1, TS_VSS2, TS_VSS3 and TS_VSS4 should not float on the motherboard. They should be tied to GND directly.

NCTF:
- TP2206 — PCH_NCTF_1 — A4 — VSS_NCTF_1#A4
- TP2212 — PCH_NCTF_7 — A45 — VSS_NCTF_3#A45
- VSS_NCTF_2#A44, VSS_NCTF_4#A46, VSS_NCTF_5#A5, VSS_NCTF_6#A6, VSS_NCTF_7#B3, VSS_NCTF_8#B47, VSS_NCTF_9#BD1, VSS_NCTF_10#BD49, VSS_NCTF_11#BE1, VSS_NCTF_12#BE49, VSS_NCTF_13#BF1, VSS_NCTF_14#BF49
- TP2207 — PCH_NCTF_2 — BE1
- TP2208 — PCH_NCTF_3 — BE49
- TP2209 — PCH_NCTF_4 — BF49
- NCTF_TEST_PINS: A4,A45,A44,A46,A5,A6,B3,B47, BD1,BD49,BE1,BE49,BF1,BF49, BG2,BG48,BH3,BH47,BJ4,BJ44, BJ45,BJ46,BJ5,BJ36,C2,C48,D1, D49,E1,E49,F1,F49
- VSS_NCTF_15#BG2, VSS_NCTF_16#BG48, VSS_NCTF_17#BH3, VSS_NCTF_18#BH47, VSS_NCTF_19#BJ4, VSS_NCTF_20#BJ44, VSS_NCTF_21#BJ45, VSS_NCTF_22#BJ46, VSS_NCTF_23#BJ5, VSS_NCTF_24#BJ36, VSS_NCTF_25#C2, VSS_NCTF_26#C48, VSS_NCTF_27#D1, VSS_NCTF_28#D49, VSS_NCTF_29#E1, VSS_NCTF_30#E49, VSS_NCTF_31#F1, VSS_NCTF_32#F49
- PCH_NCTF_9 — TP2214; PCH_NCTF_10 — TP2215; PCH_NCTF_5 — TP2210; PCH_NCTF_8 — TP2213; PCH_NCTF_6 — TP2211

1D8V_S0 — R1808 2K2R2J-2-GP — NV_CLE — R1809 1KR2J-1-GP — H_SNB_IVB# 5

DMI & FDI Termination Voltage

NV_CLE	Set to Vss when LOW Set to Vcc when HIGH

3D3V_S0 — R2207 10KR2J-3-GP — FDI_OVRVLTG — R2208 10KR2J-3-GP

FDI TERMINATION VOLTAGE OVERRIDE

GPIO37 (FDI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

3D3V_S0 — R2209 10KR2J-3-GP — DMI_OVRVLTG — R2210 10KR2J-3-GP

DMI TERMINATION VOLTAGE OVERRIDE

GPIO36 (DMI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

3D3V_S0 — R2220 10KR2J-3-GP — PCH_GPIO48; R2224 10KR2J-3-GP — FP_DET#; R2222 10KR2J-3-GP — PCH_TEMP_ALERT#

RN2201 — SRN10KJ-5-GP — EC_SMI#, EC_SCI#, DGPU_HPD_INTR#, PCH_GPIO22

R2225 10KR2J-3-GP — PSW_CLR#, MFG_MODE

R2228 10KR2J-3-GP

R2229 10KR2J-3-GP — PCH_GPIO27

3D3V_S5 — RN2204 — SRN10KJ-5-GP — RTC_DET#, USB3_PWR_ON

R2201 1KR2J-1-GP — PCH_GPIO15

R2234 10KR2J-3-GP — PLL_ODVR_EN

3D3V_S5 — R2221 10KR2J-3-GP — Gsensor_ID — R2226 10KR2J-3-GP DY

D2201 CH751H-40-L-GP — G2201 GAP-OPEN

FP_DET# — R2223 10KR2J-3-GP

	INTERNAL GFX	EXTERNAL GFX
R2205	DY	10K
R2206	100K	DY

3D3V_S0 — R2205 10KR2J-3-GP DY — GFX_CRB_DET — R2206 100KR2J-1-GP

3D3V_S0 — R2230 10KR2J-3-GP DY — R2232 10KR2J-3-GP DY — VRAM_SIZE1, VRAM_SIZE2

PLL ON DIE VR ENABLE

NOTE:This signal has a weak internal pull-up 20K
ENABLED -- HIGH (R2212 UNSTUFFED) DEFAULT
DISABLED -- LOW (R2212 STUFFED)

PLL_ODVR_EN — R2212 1KR2J-1-GP

Integrated Clock Enable functionality is achieved via soft-strap. The default is integrated clock enable.

Integrated Clock Chip Enable	
ICC_EN#	HIGH (R2211 DY) - DISABLED [DEFAULT] LOW (R2211) - ENABLED

GPIO8 has a weak [20K] internal pull up.
Integrated Clock Enable functionality is achieved via soft-strap. The default is integrated clock enable.

DY — ICC_EN# — R2211 1KR2J-1-GP

R2211 BOM CTRL
HR:1K
CRV:DY

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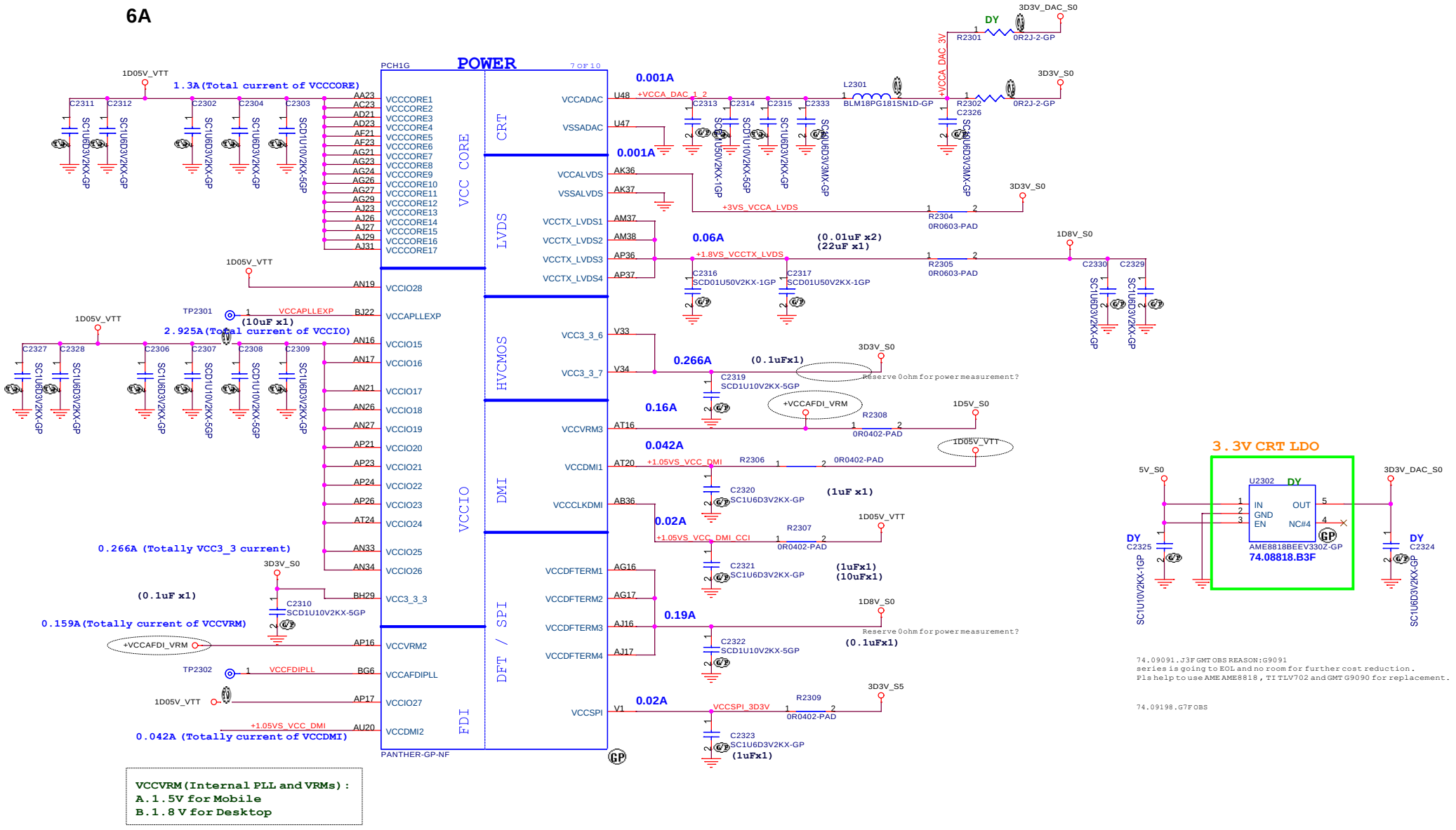
Title: PCH : GPIO/NTCF/MISC

Size	Document Number	Rev
A2	LA480	SD

Date: Friday, January 06, 2012 Sheet 22 of 103

SSID = PCH

6A



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Title: PCH : POWER1

Size: A3 | Document Number: LA480 | Rev: SD

Date: Friday, January 06, 2012 | Sheet 23 of 103

SSID = PCH

POWER

PCH1J — PANTHER-GP-NF — 10 OF 10

Clock and Miscellaneous

TP2401	VCCACLK	AD49
3D3V_S5 → 0.002A (0.1uFx1) → R2403 0R0603-PAD	+VCCPDSW	T16
TP2405	DCPSUSBYP	V12
	+V3.3S_VCC_CLKF33	T38
TP2404	+VCCAPLL_CPY_PCH	BH23
(10uFx1) 1D05V_VTT	VCCIO14	AL29
TP2402	+VCCSUS1	AL24
	DCPSUS3	

3D3V_S0 → L2401 IND-10UH-218-GP → +V3.3S_VCC_CLKF33 (10uFx1) (1uFx1)
68.10050.10Y
2nd = 68.1001E.10N
C2401 SC10U6D3V5KX-1GP, C2402 SC1U10V2KX-1GP

1D05V_M — 1.01A (Total current of VCCASW)

VCCASW1	AA19
VCCASW2	AA21
VCCASW3	AA24
VCCASW4	AA26
VCCASW5	AA27
VCCASW6	AA29
VCCASW7	AA31
VCCASW8	AC26
VCCASW9	AC27
VCCASW10	AC29
VCCASW11	AC31
VCCASW12	AD29
VCCASW13	AD31
VCCASW14	W21
VCCASW15	W23
VCCASW16	W24
VCCASW17	W26
VCCASW18	W29
VCCASW19	W31
VCCASW20	W33

C2403 SC10U6D3V3MX-GP, C2436 SC1U6D3V2KX-GP, C2437 SC1U6D3V2KX-GP, C2406 SC1U6D3V2KX-GP, C2407 SC1U6D3V2KX-GP, C2408 SC1U6D3V2KX-GP

1D05V_VTT — L2402 IND-10UH-218-GP — +1.05VS_VCCA_A_DPL — 0.08A
68.10050.10Y
2nd = 68.1001E.10N
DY
C2443 SC10U6D3V3MX-GP, C2409 SC1U6D3V2KX-GP
(1uFx1) (220uFx1)

1D05V_VTT — L2403 IND-10UH-218-GP — +1.05VS_VCCA_B_DPL — 0.08A
68.10050.10Y
2nd = 68.1001E.10N
DY
C2444 SC10U6D3V3MX-GP, C2410 SC1U6D3V2KX-GP
(1uFx1) (220uFx1)

+VCCRTCEXT	DCPRTC	N16
0.16A (Totally current of VCCVRM)		
C2411 SCD1U10V2KX-5GP (0.1uFx1)	+VCCAFDI_VRM	Y49
	VCCVRM4	
+1.05VS_VCCA_A_DPL	VCCADPLLA	BD47
+1.05VS_VCCA_B_DPL	VCCADPLLB	BF47
1D05V_VTT R2404 0R0402-PAD +VCCDIFFCLK → C2412 SC1U6D3V2KX-GP	VCCIO7	AF17
1D05V_VTT (1uFx1) R2406 0R0603-PAD +VCCDIFFCLKN → C2414 SC1U6D3V2KX-GP	VCCDIFFCLKN1	AF33
0.055A	VCCDIFFCLKN2	AE34
	VCCDIFFCLKN3	AG34
0.095A	VCCSSC	AG33
+V1.05S_SSCVCC (1uFx1)		
1D05V_VTT R2405 0R0402-PAD +V1.05S_SSCVCC → C2413 SC1U6D3V2KX-GP		
(0.1uFx1) C2415 SCD1U10V2KX-5GP	DCPSST	V16
(1uFx1) TP2406 DCPSUS	DCPSUS1	T17
	DCPSUS2	V19
1D05V_VTT R2413 0R0402-PAD	V_PROC_IO	BJ8
V_PROC_IO_R 0.001A		
(0.1uFx2) (4.7uFx1_0603) C2417 SC1U6D3V2KX-GP, C2418 SCD1U10V2KX-5GP, C2419 SCD1U10V2KX-5GP		
	VCCRTC	A22
RTC_AUX_S5 6uA		
(0.1uFx2) (1uFx1) C2416 SC1U6D3V2KX-GP, C2421 SCD1U10V2KX-5GP, C2422 SCD1U10V2KX-5GP		

USB

VCCIO29	N26	1D05V_VTT (1uFx1) C2423 SCD1U10V2KX-5GP
VCCIO30	P26	
VCCIO31	P28	
VCCIO32	T27	
VCCIO33	T29	
0.097A (Totally current of VCCSUS3_3)		
VCCSUS3_3_7	T23	3D3V_S5 (0.1uFx1) C2424 SCD1U10V2KX-5GP
VCCSUS3_3_8	T24	
VCCSUS3_3_9	V23	
VCCSUS3_3_10	V24	
VCCSUS3_3_6	P24	3D3V_S5 (0.1uFx1) C2425 SCD1U10V2KX-5GP
VCCIO34	T26	1D05V_VTT
V5REF_SUS	M26	+5VA_PCH_VCC5REFSUS 0.001A
DCPSUS4	AN23	+VCCA_USBSUS → TP2403
VCCSUS3_3_1	AN24	3D3V_S5

3D3V_S5 → D2401 CH751H-40PT-GP 83.R0304.A8F 2nd = 83.R2004.B8F → R2408 10R2J-2-GP → 5V_S5 (0.1uFx1) C2426 SCD1U10V2KX-5GP

3D3V_S0 → D2402 CH751H-40PT-GP 83.R0304.A8F 2nd = 83.R2004.B8F → R2407 10R2J-2-GP → 5V_S0 (1uFx1) C2427 SC1U10V2KX-1GP

PCI/GPIO/LPC

V5REF	P34	+5VS_PCH_VCC5REF 0.001A
VCCSUS3_3_2	N20	3D3V_S5 (1uFx1)
VCCSUS3_3_3	N22	C2428 SC1U6D3V2KX-GP
VCCSUS3_3_4	P20	
VCCSUS3_3_5	P22	
VCC3_3_1	AA16	3D3V_S0 (0.1uFx2) C2430 SCD1U10V2KX-5GP, C2431 SCD1U10V2KX-5GP
VCC3_3_8	W16	
VCC3_3_4	T34	
VCC3_3_2	AJ2	3D3V_S0 (0.1uFx1) C2429 SCD1U10V2KX-5GP

SATA

VCCIO5	AF13	
VCCIO12	AH13	1D05V_VTT (1uFx1) C2432 SC1U6D3V2KX-GP
VCCIO13	AH14	
VCCIO6	AF14	
VCCAPLLSATA	AK1	+V1.05S_VCCAPLL_SATA3 → TP2407
VCCVRM1	AF11	+VCCAFDI_VRM
VCCIO2	AC16	
VCCIO3	AC17	1D05V_VTT (1uFx1) C2435 SCD1U10V2KX-5GP
VCCIO4	AD17	

MISC

1D05V_M		
VCCASW22	T21	
VCCASW23	V21	
VCCASW21	T19	

HDA

VCCSUSHDA	P32	0.01A +3VS_+1.5VS_HDA_IO (0.1uFx1) C2433 SCD1U10V2KX-5GP

+3VS_+1.5VS_HDA_IO → R2409 0R0603-PAD → 3D3V_S5

<Core Design>

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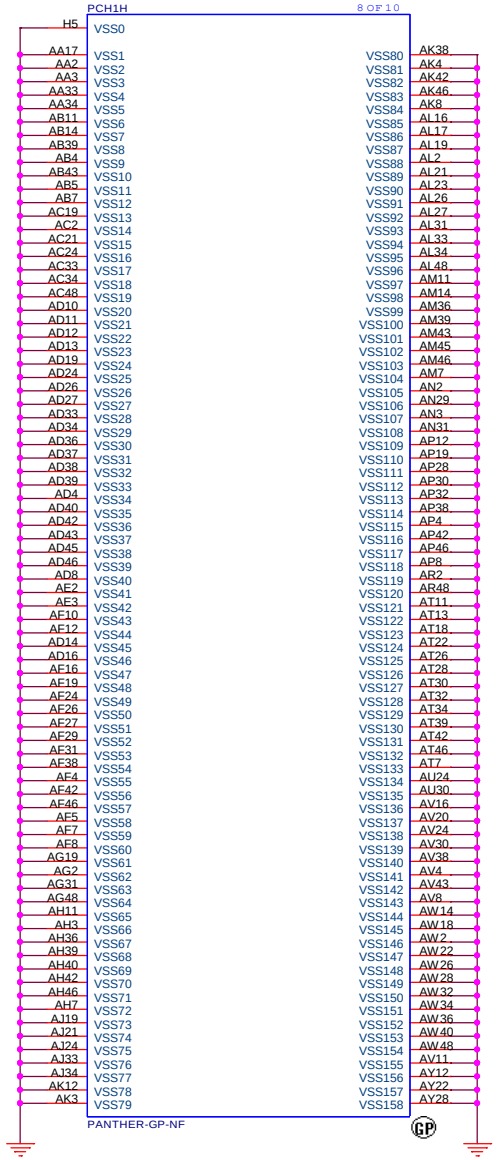
Taipei Hsien 221, Taiwan, R.O.C.

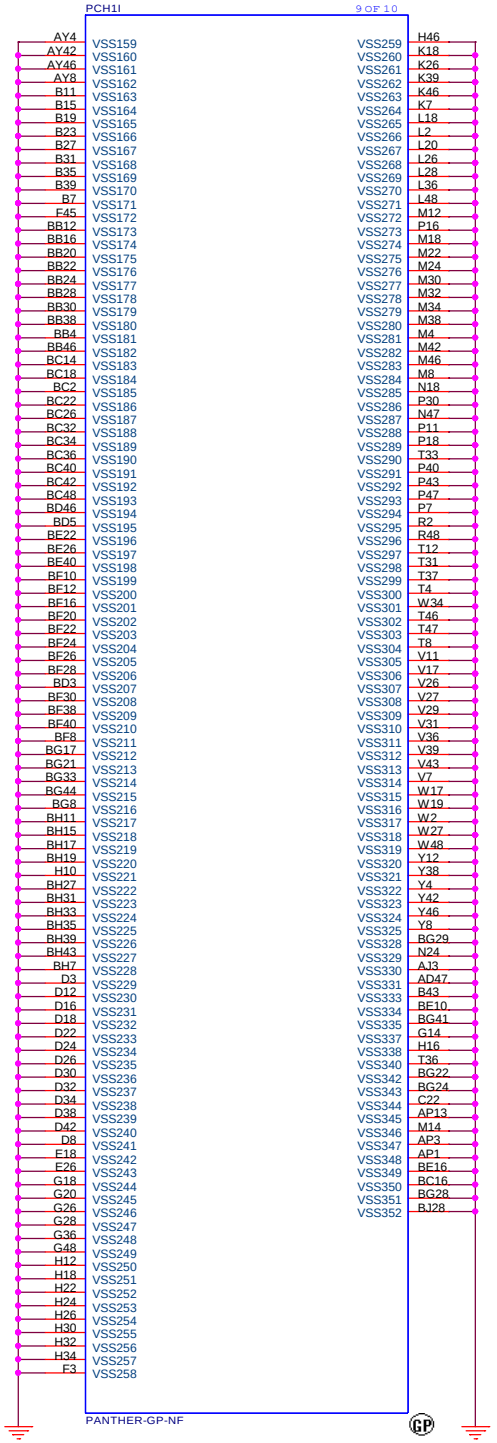
Title: **PCH : POWER2**

Size	Document Number	Rev
A3	LA480	SD

Date: Friday, January 06, 2012 Sheet 24 of 103

SSID = PCH





<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***PCH : VSS***

Size	Document Number	Rev
A3	LA480	SD

Date: Friday, January 06, 2012 Sheet 25 of 103

BLANK

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title
Reserved

Size	Document Number	Rev
A4	**LA480**	**SD**

Date: Friday, January 06, 2012 Sheet 26 of 103

SSID = KBC

65W: 1.7V
90W: 3.3V

Code change to Low Active on 8/19

EC_GPIO47 High Active

Reset IC: Prevent BIOS data loss solution

EC GPIO standard PH/PL

MODEL_ID_AD (Pin100)	Pull Down	Pull High	Voltage
UMA	100.0K	33.0K	2.481V
OPTIMUS	100.0K	47.0K	2.245V

PCB Version A/D (Pin98)	Pull-Low Resistor	Pull-High Resistor (3D3V_AUX_S5)	Voltage
SA	100.0K	10.0K	3.0V
SB	100.0K	20.0K	2.75V
SC	100.0K	33.0K	2.48V
-1	100.0K	47.0K	2.24V
Reserved	100.0K	64.9K	2.0V
Reserved	100.0K	76.8K	1.87V
Reserved	100.0K	100.0K	1.65V

71.00885.A0G
IC EMB CTRL NPCE885PA0DX LQFP 128P

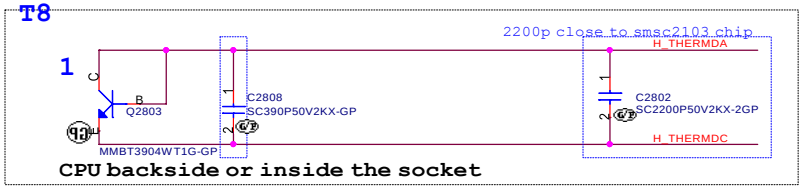
Wistron Corporation

SSID = Thermal

Thermal sensor

20110718_Carrey:
For Vendor suggestion, add 390pF Cap. as closed to pin B/C and E of Q2803

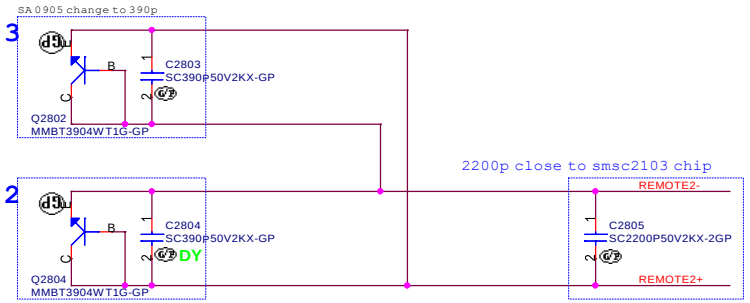
T8



CPU backside or inside the socket

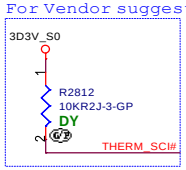
CPU TEMP:
H_THERMDA and H_THERMDC routing 10mil trace width and spacing. Locate Capacity near Thermal diode.

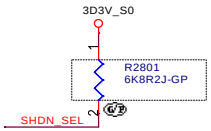
Close to SO-DIMM on top side.



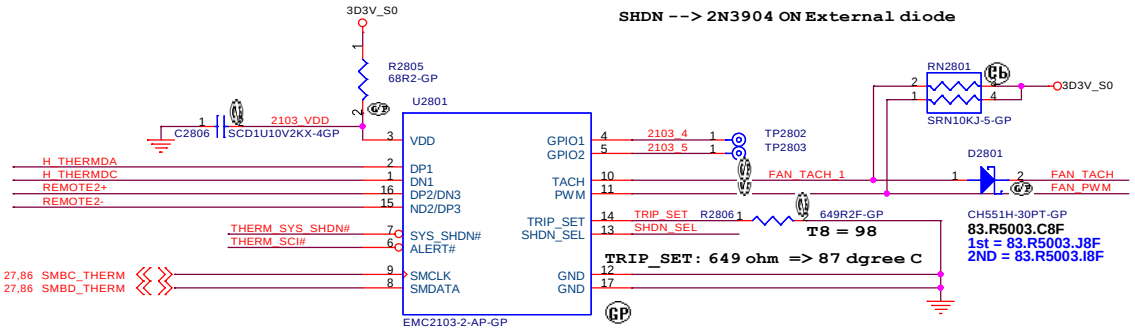
between CPU, VGA and DIMM on bottom side

20110718_Carrey:
For Vendor suggestion, add 10k pull high to 3D3V_S0



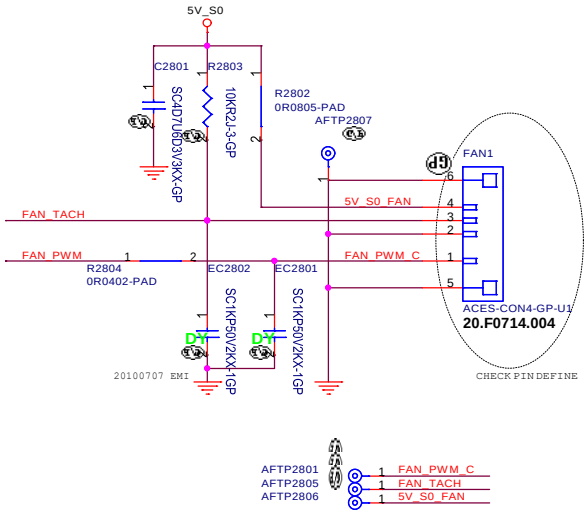


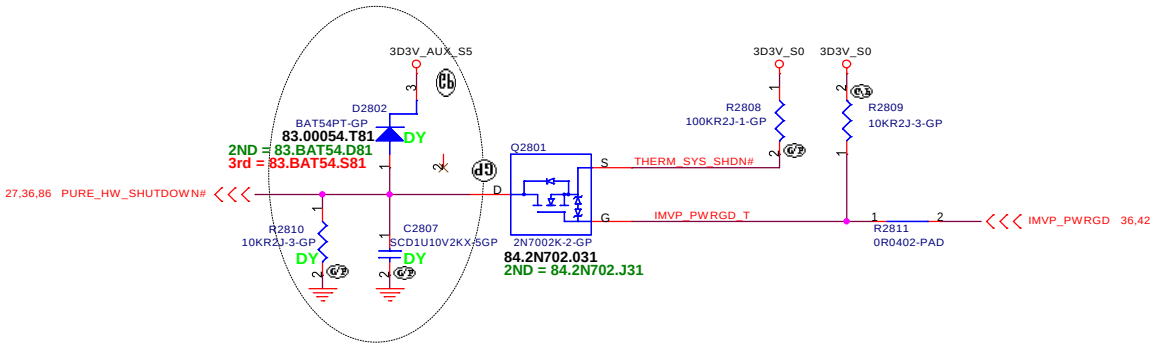
SHDN --> 2N3904 ON External diode



pin6, ALERT# OD
pin7, SYS_SHDN# OD

4 WIRE PWM Fan Control circuit





<Core Design>

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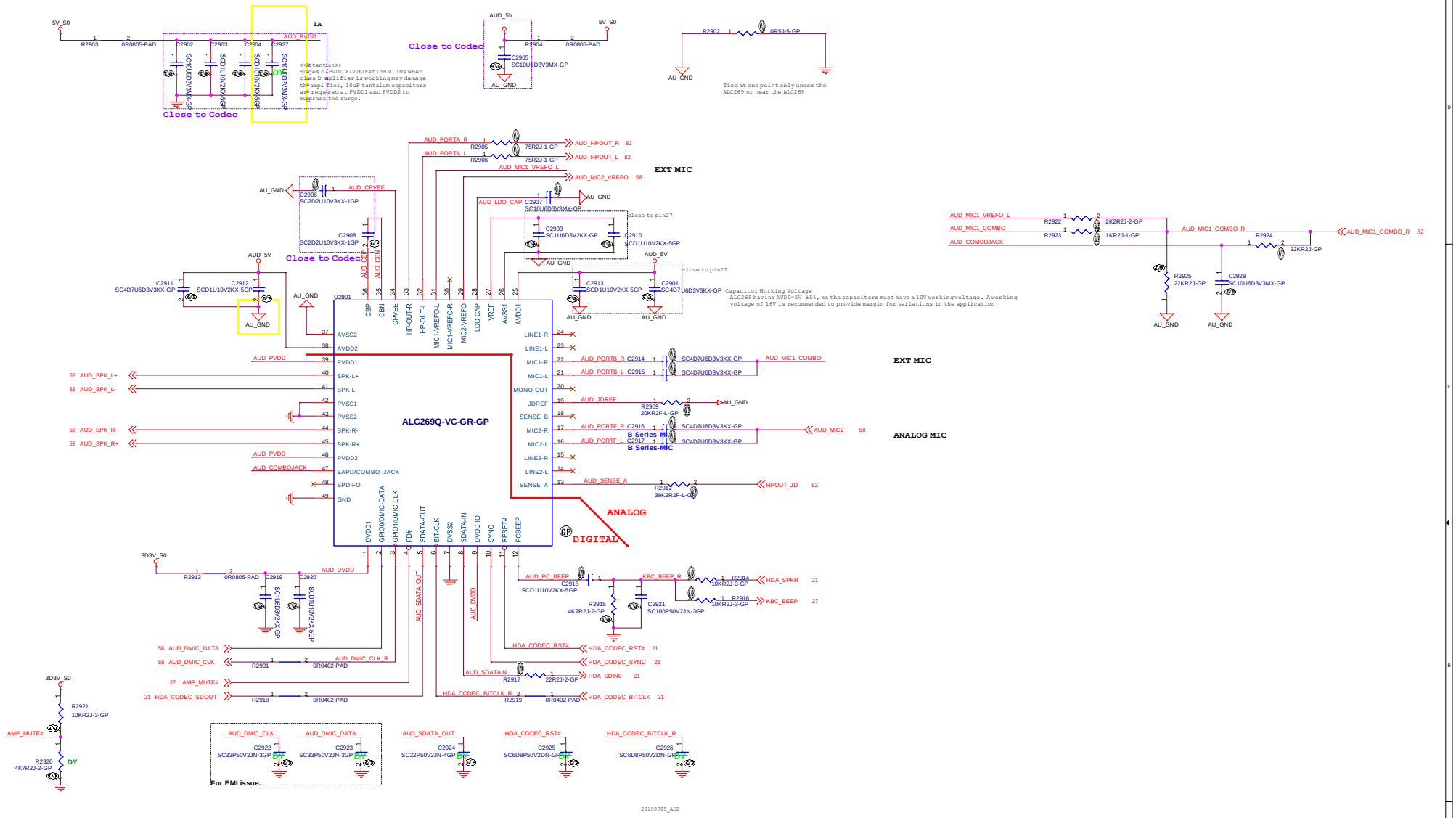
Taipei Hsien 221, Taiwan, R.O.C.

Title: THERMAL SENSOR SMSC EMC2103

Size	Document Number	Rev
A3	LA480	SD

Date: Friday, January 06, 2012 Sheet 28 of 103



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **AUDIO CODEC**

Size	Document Number	Rev
A2	LA480	SD

Date: Friday, January 06, 2012 Sheet 29 of 103

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<Core Design>

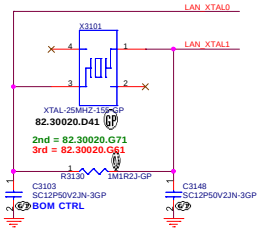
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	LA480	SD

Date: Friday, January 06, 2012 Sheet 30 of 103

25MHz XTAL

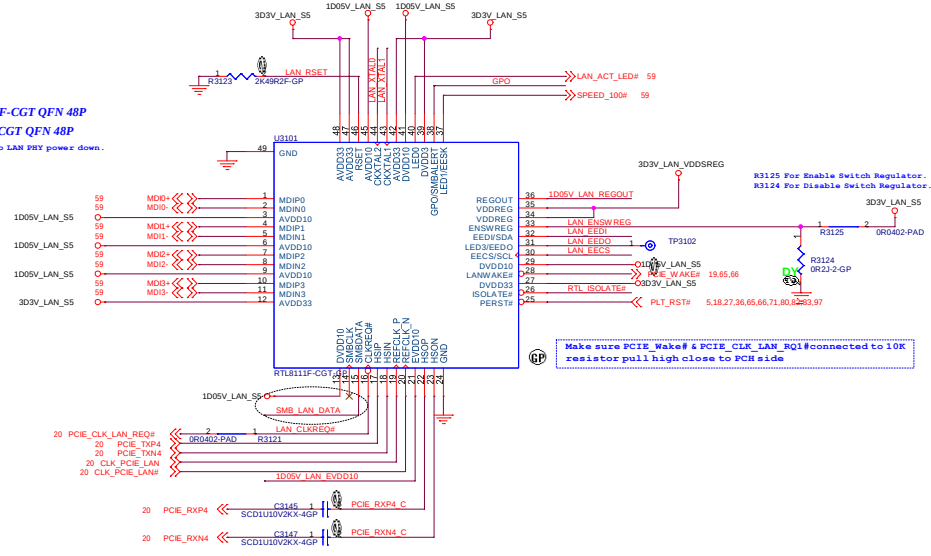


	C3103	C3148
VB480	15pF 78.15034.1FL	12pF
VB580	12pF 78.12034.1FL	12pF

71.08111.N03, IC PCIE CTRL RTL8111F-CGT QFN 48P

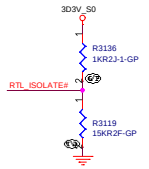
71.08111.J03, IC PCI-E RTL8111E-VL-CGT QFN 48P

8111F can use GPIO to inform system to do LAN PHY power down.

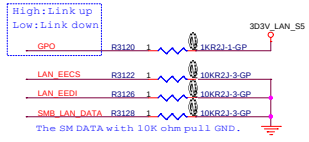


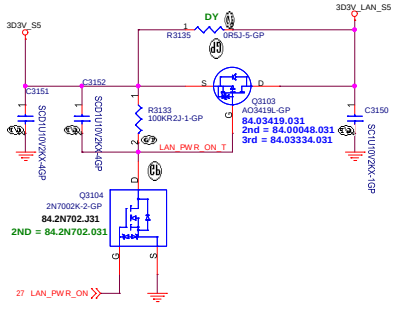
Make sure PCIE_Wake# & PCIE_CLK_LAN_RQ1# connected to 10K resistor pull high close to PCH side

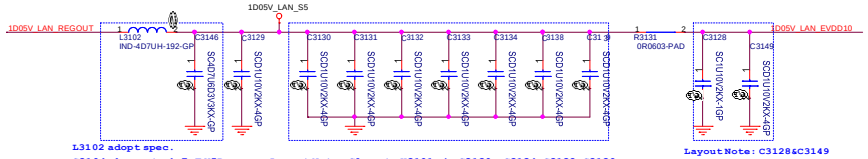
main pwr if have no ASF



High:Link up
Low:Link down



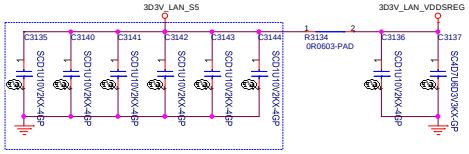




L3102 adopt spec.
C3104 change to 4.7uF X5R type capacitor

Layout Note: Close to U3101 pin C3130 ~ C3134,C3138,C3139 For VDD10 pins - 3, 6, 9, 13, 29, 41, 45.

Layout Note: C3128&C3149 Close to U3101 pin21



Layout Note: C3135, C3140~C3144 Close to U3101 pin For VDD33 pins - 12, 27, 39, 42, 47, 48.

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: LAN_RTL8111F

Size: A2 | Document Number: LA480 | Rev: SD

Date: Friday, January 06, 2012 | Sheet 31 of 103

<Core Design>

緯創資通 Wistron Corporation
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Title

R5U220 (CARD READER)

Size	Document Number	Rev
A1	LA480	SD

Date: Friday, January 06, 2012 Sheet 30 of 39

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<Core Design>

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	LA480	SD

Date: Friday, January 06, 2012 Sheet 33 of 103

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<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title
Reserved

Size	Document Number	Rev
A4	**LA480**	**SD**

Date: Friday, January 06, 2012 Sheet 34 of 103

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<Core Design>

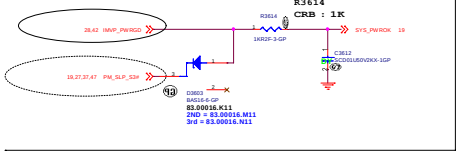
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***USB 3.0 Controller***

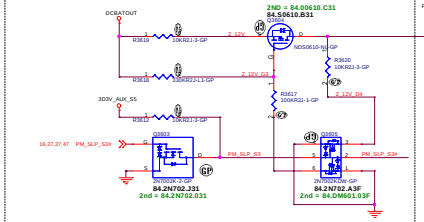
Size	Document Number	Rev
A4	LA480	SD

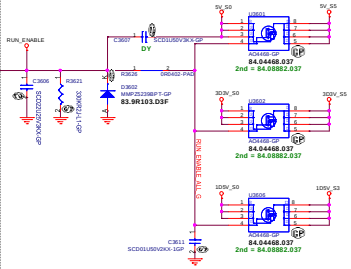
Date: Friday, January 06, 2012 Sheet 35 of 103

Power Sequence



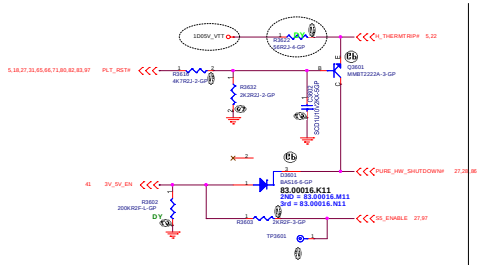
Run Power

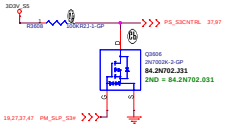




1D5V_S0

MAX Current 3000 mA
Design Current 2100 mA
Total=11.39A





<Core Design>
緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: **Power Plane Enable**

Size	Document Number	Rev
A1	LA480	SD

Date: Friday, January 05, 2007 Sheet 36 of 98

Close to CPU
S3 Power Reduction Circuit Processor VREF_DQ Implementation

DEL R3714
R3705 ->100K
DY C3701

FROM M1 /M3

12 +V_SM_VREF

R3707 1 DY 0R2J-2-GP

Q3708
2N7002K-2-GP
84.2N702.J31
2ND = 84.2N702.031

R3705 100KR2J-1-GP

C3701 SCD1U10V2KX-4GP DY

+V_SM_VREF_CNT 9

PM_SLP_S3# 19,27,36,47

Close to DIMM
S3 Power Reduction Circuit SM_DRAMPWROK

0D75V_S0
R3703 22R2J-2-GP
Q3701 DY
2N7002K-2-GP
84.2N702.J31
2ND = 84.2N702.031
36,97 PS_S3CNTRL

1D5V_S0
R3704 220R2J-L2-GP DY
Q3702 DY
2N7002K-2-GP
84.2N702.J31
2ND = 84.2N702.031
PS_S3CNTRL

SM_DRAMPWROK must have a maximum of 15ns rise or fall time over VDDQ * 0.55± 200mV and the edge must be monotonic

Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK

3D3V_S5
R3713 200R2F-L-GP
add 0.1uF
U3701
IN B VCC
IN A
GND OUT Y
74VHC1G09DFT2G-GP
19 PM_DRAM_PW RGD
R3715
PM_DRAM_PWRGD_R
0R0402-PAD
0D75V_EN
C3704 SCD1U10V2KX-5GP DY
OD AND gate required
73.01G09.AAH
2nd = 73.01G09.0AB
3rd = 73.01G09.BAH
VDDPWRGOOD_R
1D5V_S0
R3708 200R2F-L-GP
R3719 130R2F-1-GP
VDDPWRGOOD 5
R3722 39R2J-L-GP DY
R3720 0R2J-2-GP DY
VDDPWRGOOD_D
36,97 PS_S3CNTRL
Q3707 DY
2N7002K-2-GP
84.2N702.J31
2ND = 84.2N702.031

Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK

1D5V_S3
R3706 1KR2F-3-GP
R3709 1 DY 0R2J-2-GP
S3 Power Reduction Circuit
SM_DRAMRST#
5 SM_DRAMRST#
R3711 0R0402-PAD
SM_DRAMRST#_R
Q3703
2N7002K-2-GP
84.2N702.J31
2ND = 84.2N702.031
R3701 4K99R2F-L-GP DY
SM_DRAMRST#_D
R3712 1KR2F-3-GP
DDR3_DRAMRST# 14,15
C3702 SC100P50V2JN-3GP DY
DRAMRST_CNTRL_PCH 12,20
C3703 SCD047U16V2KX-1-GP

5 S3 Power Reduction

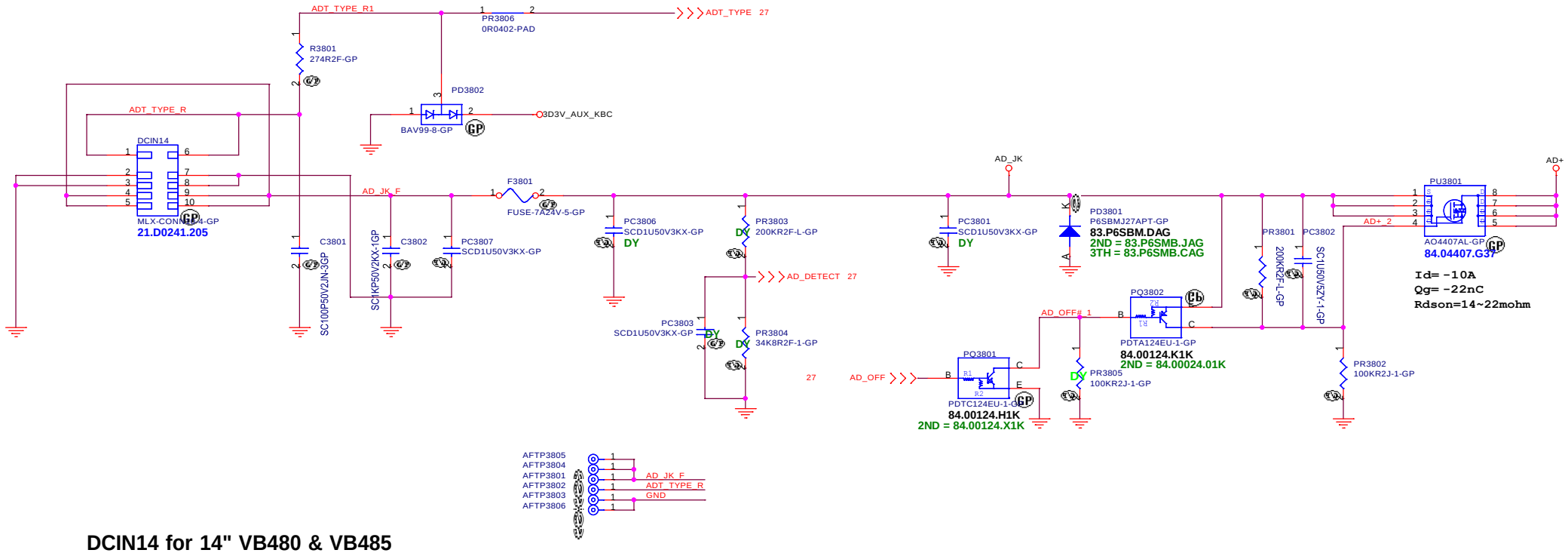
36,97 PS_S3CNTRL
Q3704
2N7002K-2-GP
84.2N702.J31
2ND = 84.2N702.031
0D75V_EN
1.05VTT_PWRGD 45,48
R3710 0R0402-PAD
19,27,36,47 PM_SLP_S3#
R3716 DY 22R2J-2-GP
0D75V_EN 46
C3705 SCD1U10V2KX-5GP DY

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ADAPTER
Size: A3
Document Number: LA480
Rev: SD
Date: Friday, January 06, 2012
Sheet 37 of 103

Adaptor in to generate DCBATOUT



DCIN14 for 14" VB480 & VB485
DCIN15 for 15" VB580 & VB585

<Core Design>

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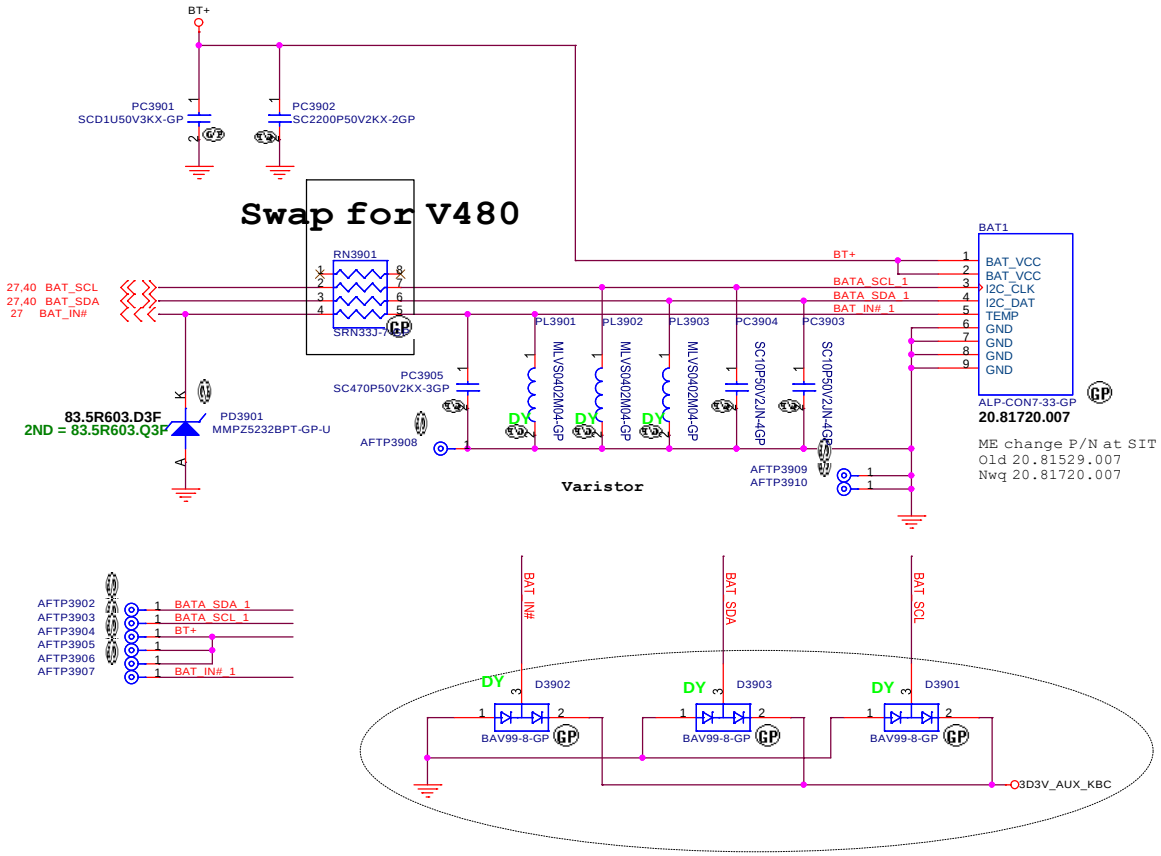
Title: *DCIN_JACK*		
Size: A3	Document Number: **LA480**	Rev: **SD**
Date: Friday, January 06, 2012	Sheet 38 of 103	

BATTERY CONNECTOR



DY on LAB stage

<Core Design>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *BATT_CONN*		
Size	Document Number: **LA480**	Rev: **SD**
Date: Friday, January 06, 2012	Sheet 39 of 103	

SSID = Charger

A8 (ANNIE/ASTRO)
PR4007,PR4008

AD+ total power	R1	R2
65w	12.4K 64.12425.6DL	100K
80w	41.2k	100K
90w	60.4k 64.60425.6DL	100K
120w	118k	100K

STOP_CHG# connects to KBC

BOM CTRL

Id= -10A
Qg= -22nC
Rdson=14~22mohm

84.04407.G37

68.00143.041

84.2N702.A3F
2nd = 84.DM601.03F

84.2N702.E31
2ND = 84.2N702.D31

1st = 83.R2003.P8F
2nd = 83.1R003.N8F
3rd = 83.R2003.B8M

Charger Current=1.4~3.6A

BQ24737RGRR-GP

<Core Design>

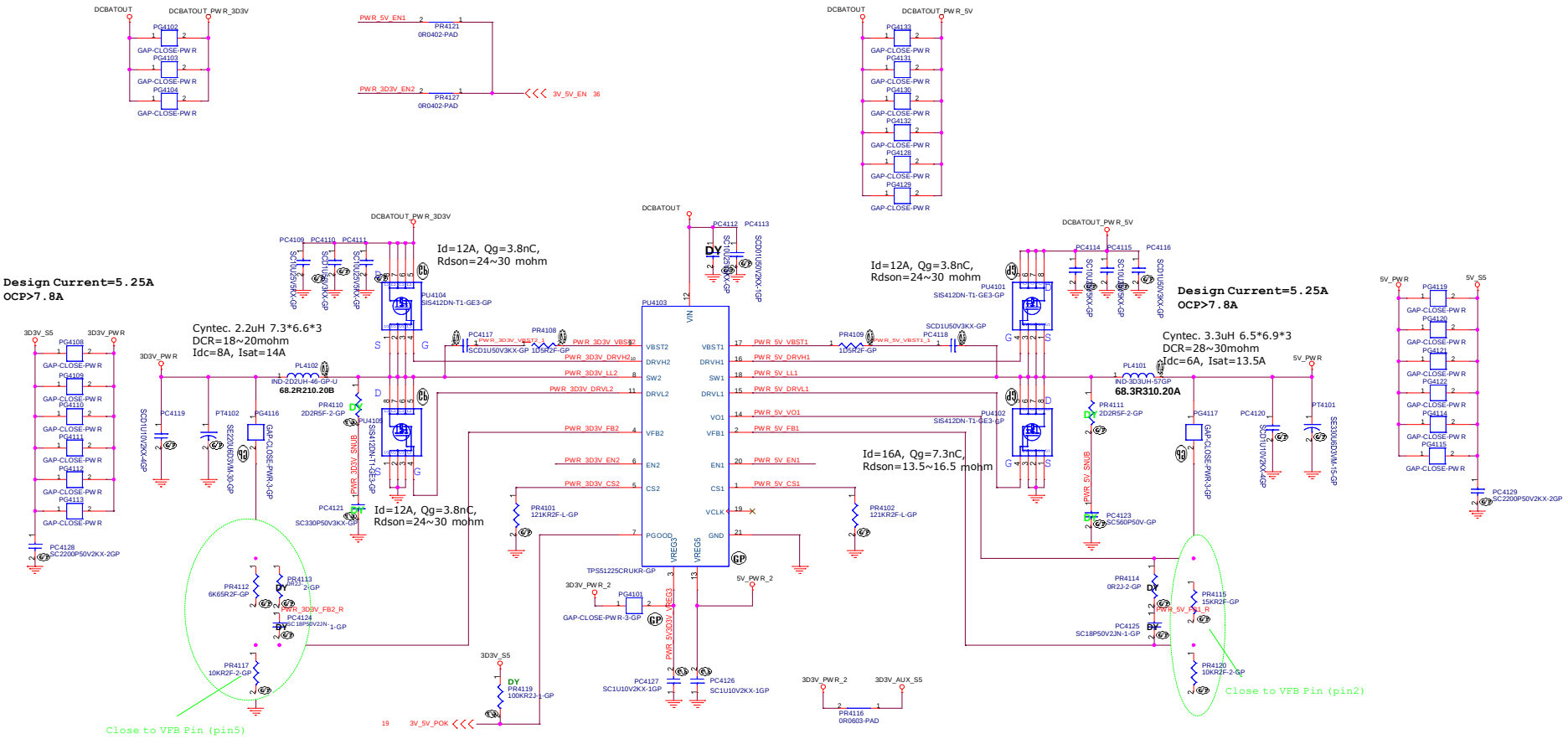
Wistron Corporation
21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih,
Taipei Hsien 221, Taiwan, R.O.C

Title: <Title>

Size: A2 | Document Number: LA480 | Rev: SD

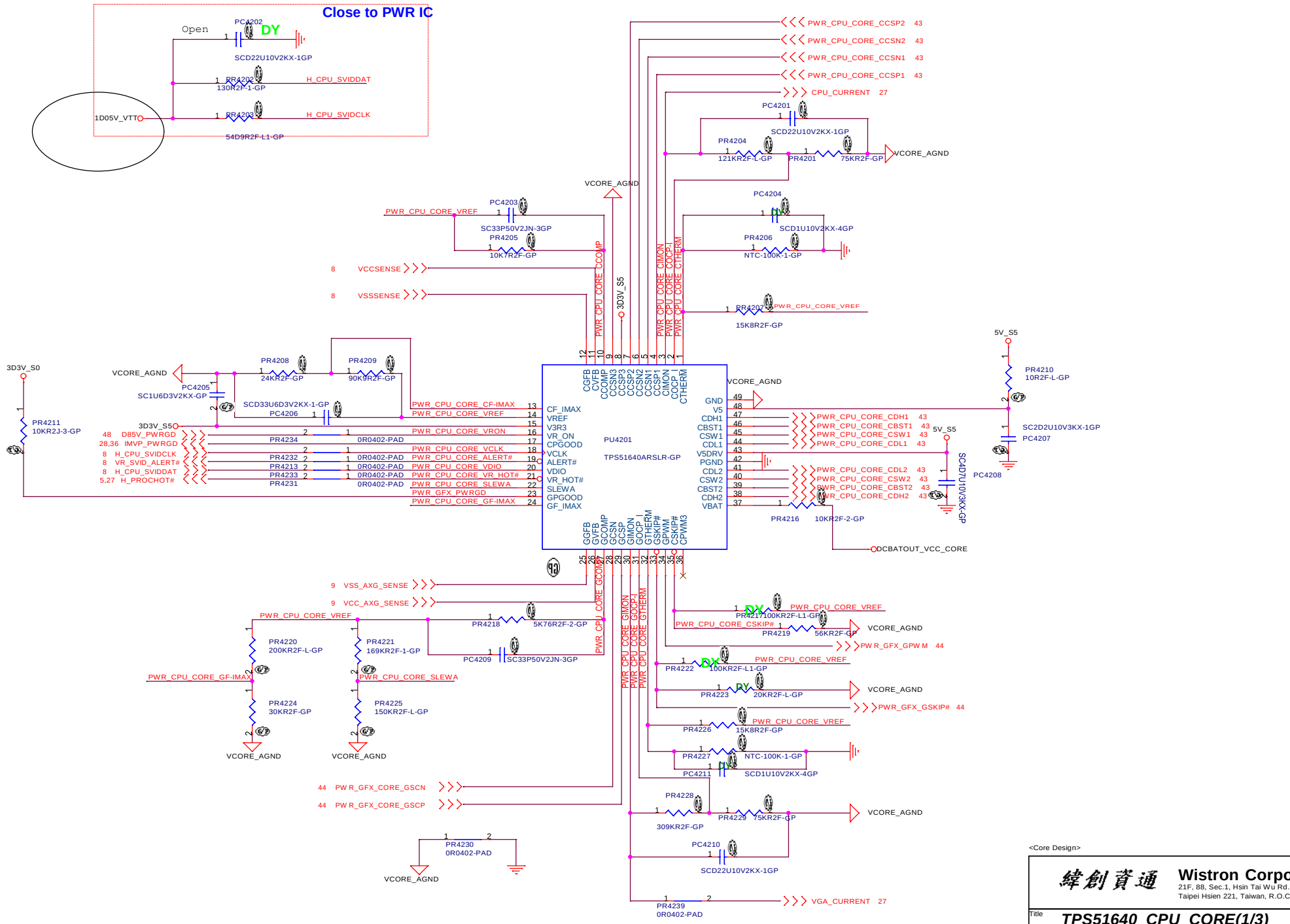
Date: Friday, January 06, 2012 | Sheet 40 of 103

SSID = PWR.Plane.Regulator_5v3p3v



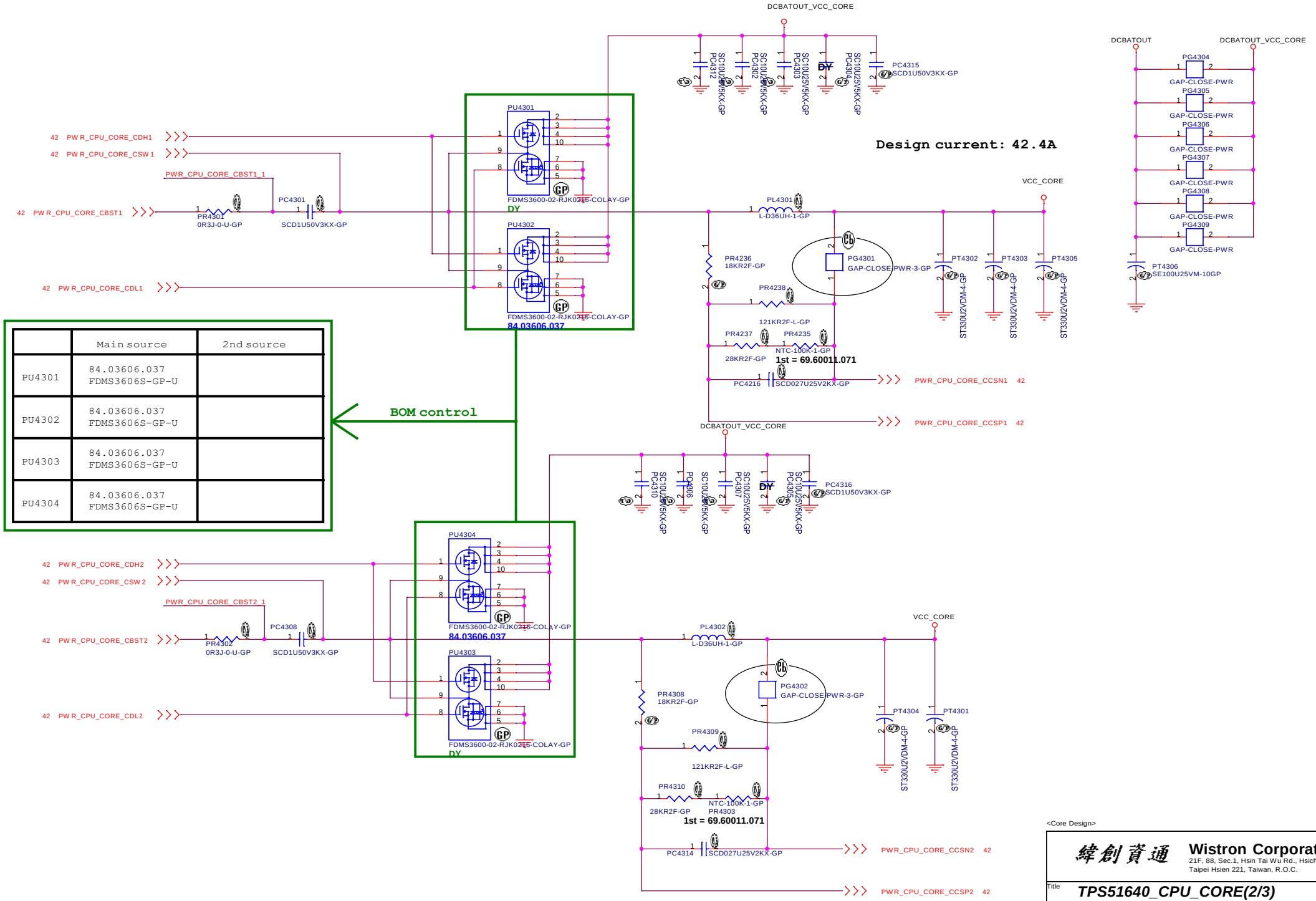
<Core Design>

緯創資通 Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	TPS51123_5V_3D3V
Size	Document Number / Rev SD
Date: Friday, January 06, 2012	Sheet 41 of 103



<Core Design>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title	TPS51640_CPU_CORE(1/3)	
Size	Document Number <Doc>	Rev SD
Date: Friday, January 06, 2012	Sheet 42 of 103	



	Main source	2nd source
PU4301	84.03606.037 FDMS3606S-GP-U	
PU4302	84.03606.037 FDMS3606S-GP-U	
PU4303	84.03606.037 FDMS3606S-GP-U	
PU4304	84.03606.037 FDMS3606S-GP-U	

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51640_CPU_CORE(2/3)

Size | Document Number: <Doc> | Rev: SD

Date: Friday, January 06, 2012 | Sheet 43 of 103

	Main source	2nd source
PU4402	84.07608.037 FDMS7608S-GP	
PU4403	84.07608.037 FDMS7608S-GP	

BOM control

DCBATOUT

DCBATOUT_VCC_GFXCORE

PG4401 GAP-CLOSE-PWR
PG4402 GAP-CLOSE-PWR
PG4403 GAP-CLOSE-PWR
PG4404 GAP-CLOSE-PWR

PU4402
PU4403
FDMS3600-02-RJK0215-COLAY-GP
84.07608.037

PWR_GFX_CORE_DRVH
PWR_GFX_CORE_SW
PWR_GFX_CORE_BST
PWR_GFX_CORE_DRVL

PR4401 0R3J-0-U-GP
PWR_GFX_CBST1_1
PC4401 SC1U25V3KX-1-GP

PC4409 SC10U25V5KX-GP
PC4402 SC10U25V5KX-GP
PC4403 SC10U25V5KX-GP
PC4404 SC10U25V5KX-GP
PC4410 SCD1U50V3KX-GP

Design current: 22A

PL4401 L-D36UH-1-GP
VCC_GFXCORE

PR4410 18KR2F-GP
PG4303 GAP-CLOSE-PWR-3-GP
PR4407 121KR2F-L-GP
PR4405 28KR2F-GP
PR4409 NTC-100K-1-GP
1st = 69.60011.071

PT4401 PT4402 PT4403 ST330U2VDM-4-GP

PC4408 SCD022U25V2KX-GP
PWR_GFX_CORE_GSCN 42
PWR_GFX_CORE_GSCP 42

PU4401 TPS51601DRBR-GP
BST SKIP# PWM GND GND DRVH SW VDD DRVL
PWR_GFX_CORE_BST
42 PWR_GFX_GSKIP#
42 PWR_GFX_GPWM
PWR_GFX_CORE_DRVH
PWR_GFX_CORE_SW
PWR_GFX_CORE_DRVL

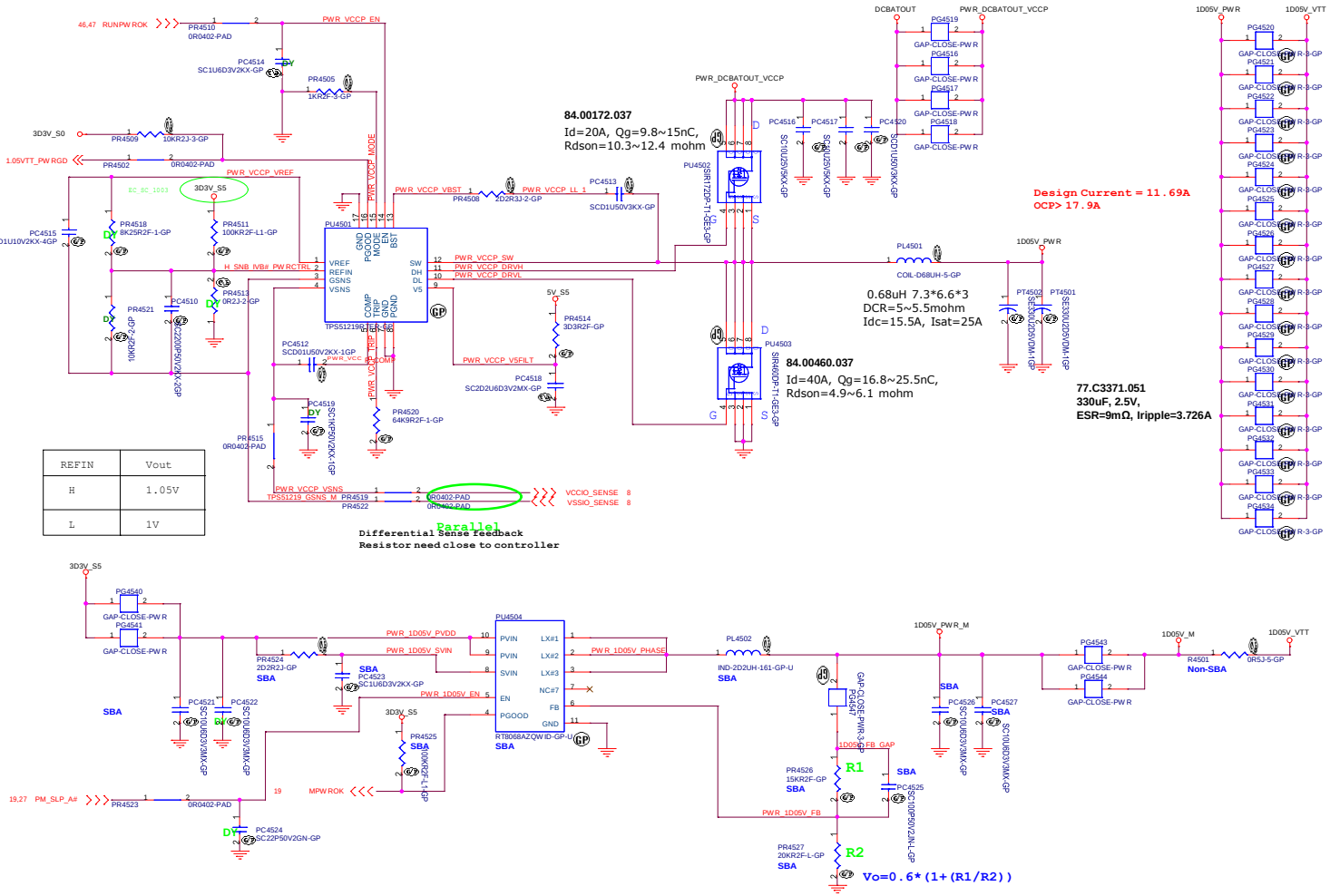
5V_S5
PC4407 SC2D2U10V3KX-1GP

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51640_CPU_CORE(3/3)
Size: Document Number: <Doc> Rev: SD
Date: Friday, January 06, 2012 Sheet 44 of 103

TPS51219 for 1D05V



REFIN	Vout
H	1.05V
L	1V

<Core Design>

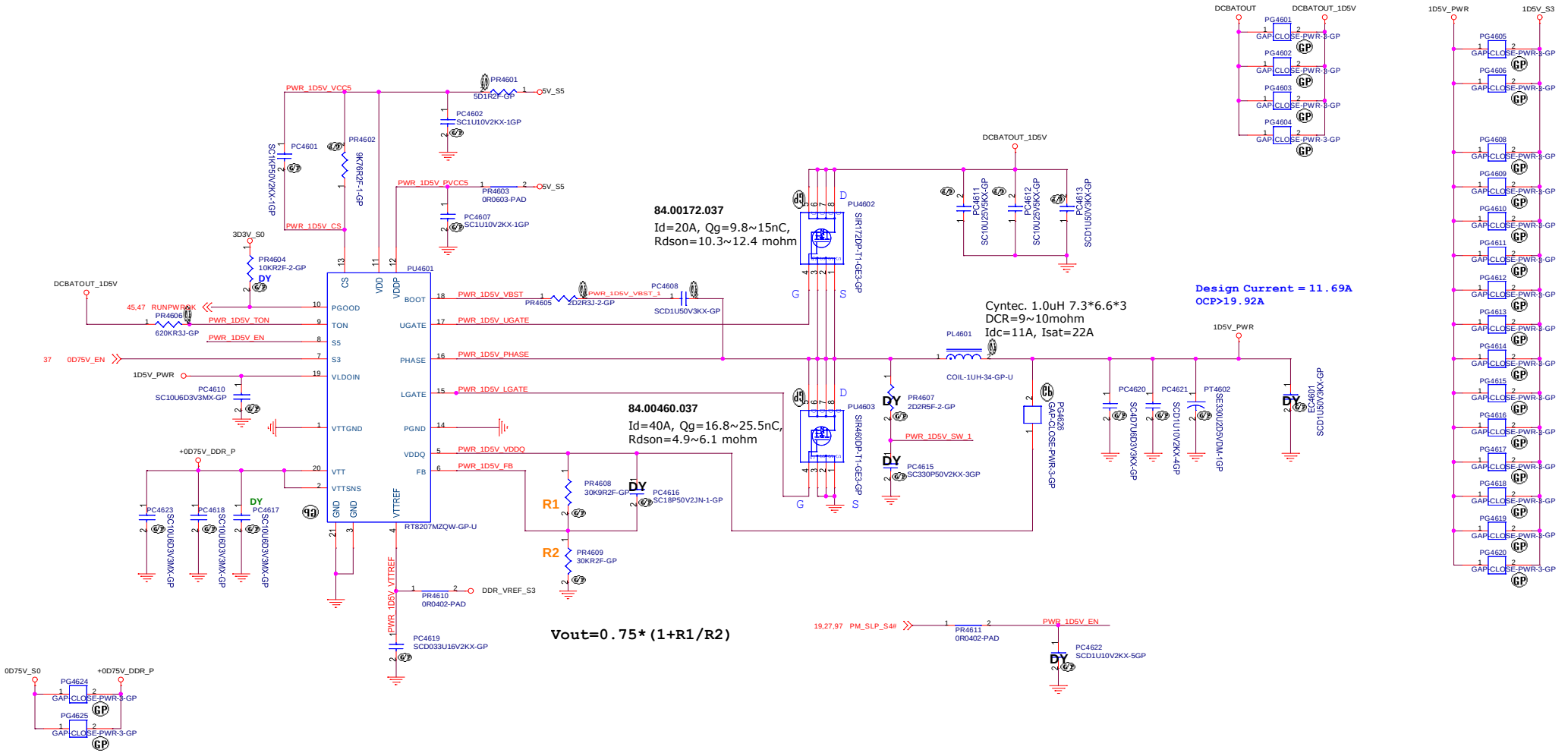
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51211_1D05V

Size: | Document Number: | Rev: SD

Date: Friday, January 06, 2012 | Sheet 45 of 103

SSID = PWR.Plane.Regulator_1p5v0p75v



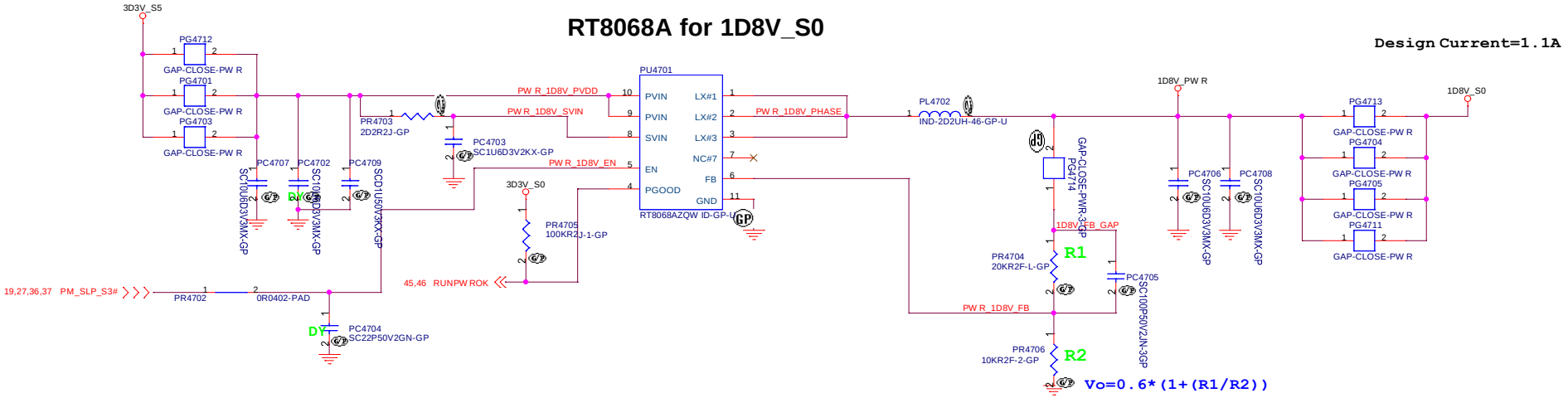
<Core Design>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: RT8207M_1D5V_0D75V		
Size	Document Number: <Doc>	Rev: SD
Date: Friday, January 06, 2012	Sheet 46 of 103	

SSID = PWR.Plane.Regulator_1p8v

RT8068A for 1D8V_S0

Design Current=1.1A



<Core Design>

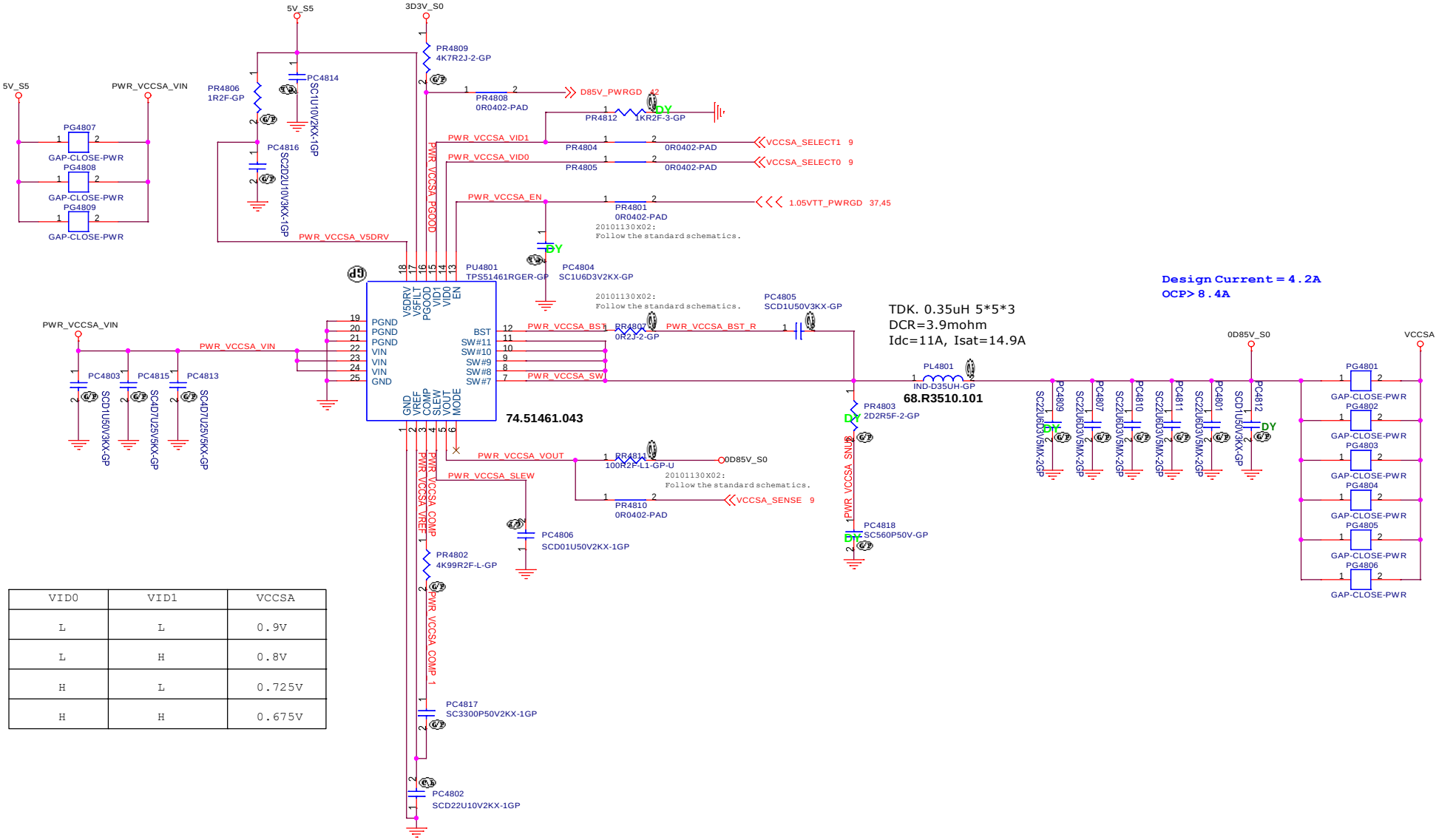
Wistron Corporation
21F, 88, Sec.1, Hsin Tai W u Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *PWM_1D8V_RT8015B*

Size	Document Number	Rev
		SD

Date: Friday, January 06, 2012 Sheet 47 of 103

TPS51461 for VCCSA



VID0	VID1	VCCSA
L	L	0.9V
L	H	0.8V
H	L	0.725V
H	H	0.675V

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: VCCSA_TPS51461

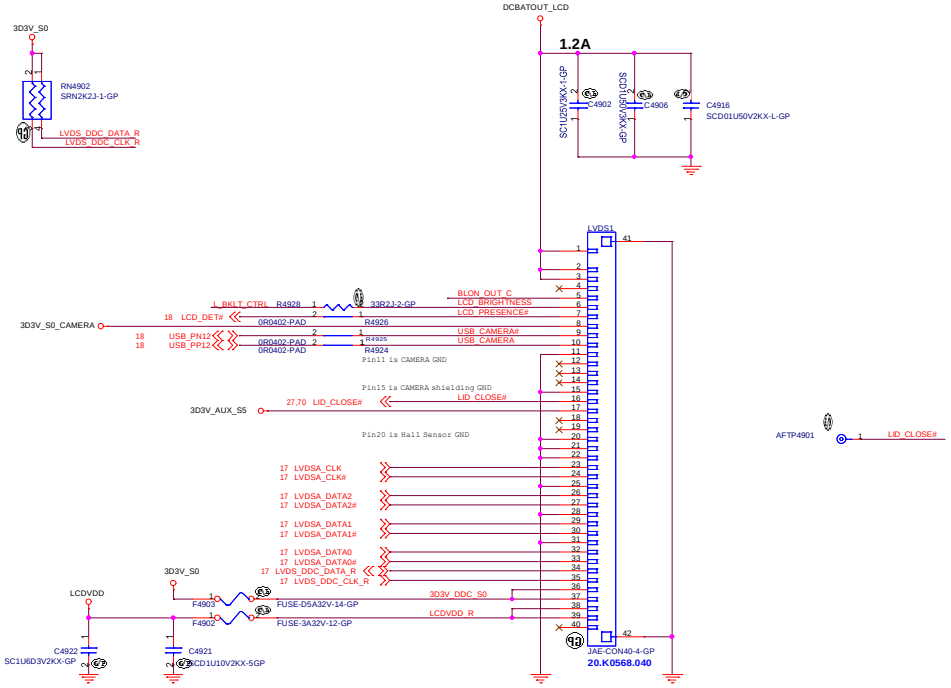
Size | Document Number: <Doc> | Rev: SD

Date: Friday, January 06, 2012 | Sheet 48 of 103

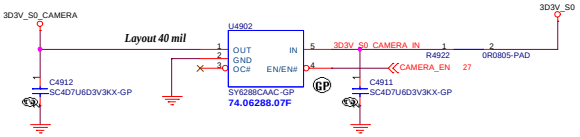
SSID = VIDEO

LVDS connector

LCD / Inverter Connector

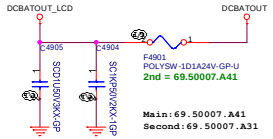


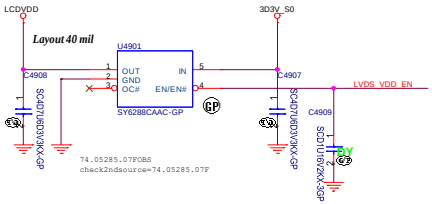
CAMERA POWER

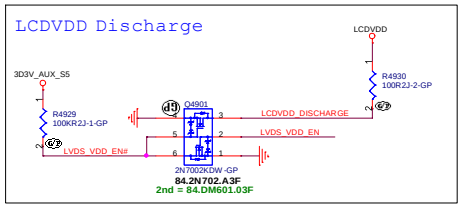


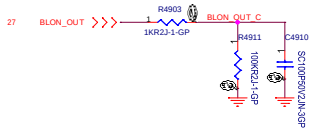
SILERGY	74.06288.07F	SY6288CAAC	High Active
DIODES	74.02171.07F	AP2171WG-7	High Active
UPI	74.07534.A7F	OBS	High Active
GMT	74.05240.A7F	OBS	High Active

LCD POWER

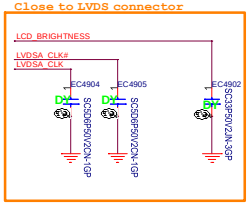




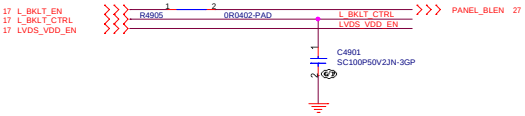




For EMI request
Close to LVDS connector



Panel BL brightness/Power En/BL En



<Core Design>

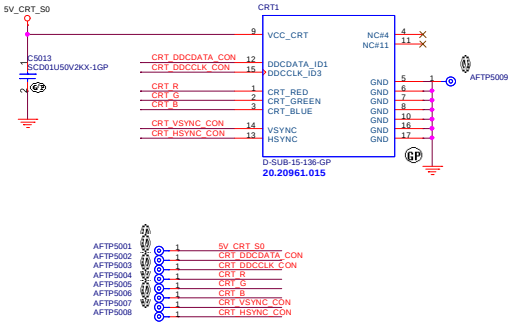
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LCD Connector

Size: A2 | Document Number: LA480 | Rev: SD

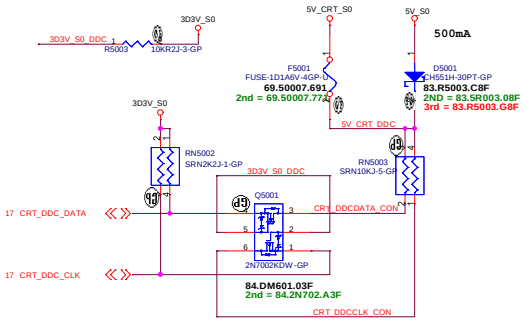
Date: Friday, January 06, 2012 | Sheet 49 of 103

CRT connector

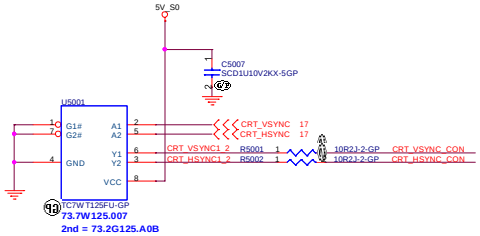


CRT DDCDATA & DDCCLK level shift

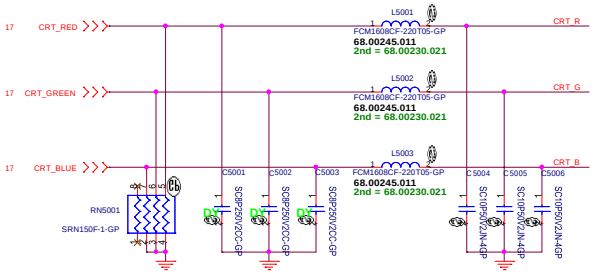
Pull High 5V Design on CRT Board

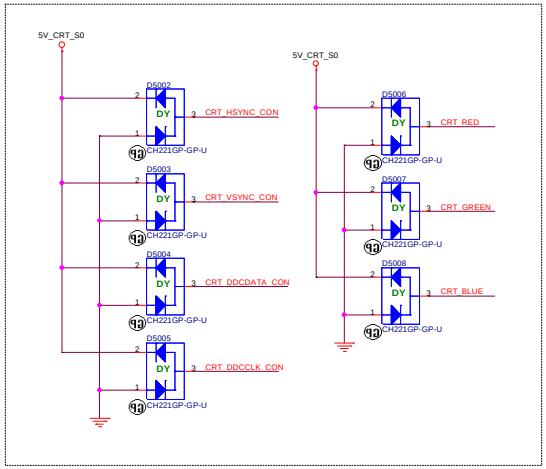


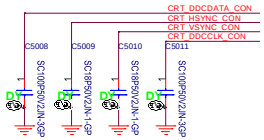
CRT Hsync & Vsync level shift



CRT RGB







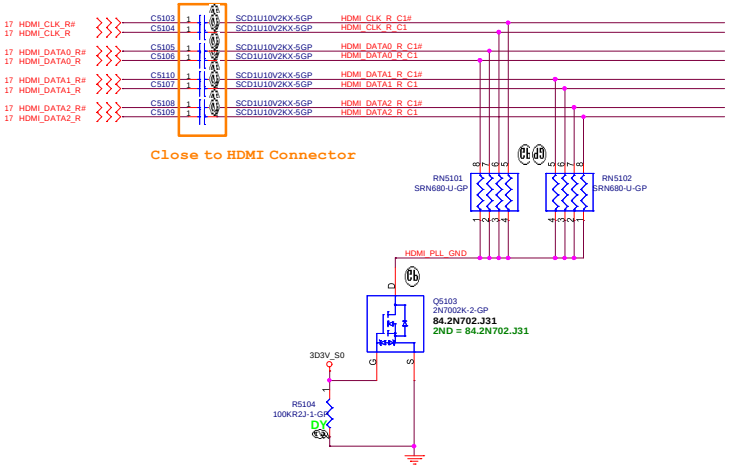
<Core Design>

緯創資通 Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title: CRT Connector	
Size: A2	Document Number: LA480
Rev: SD	
Date: Friday, January 06, 2012	Sheet 50 of 103

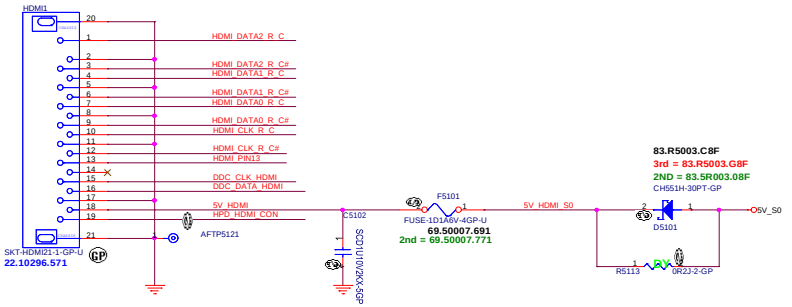
SSID = VIDEO

HDMI Passive Level Shifter

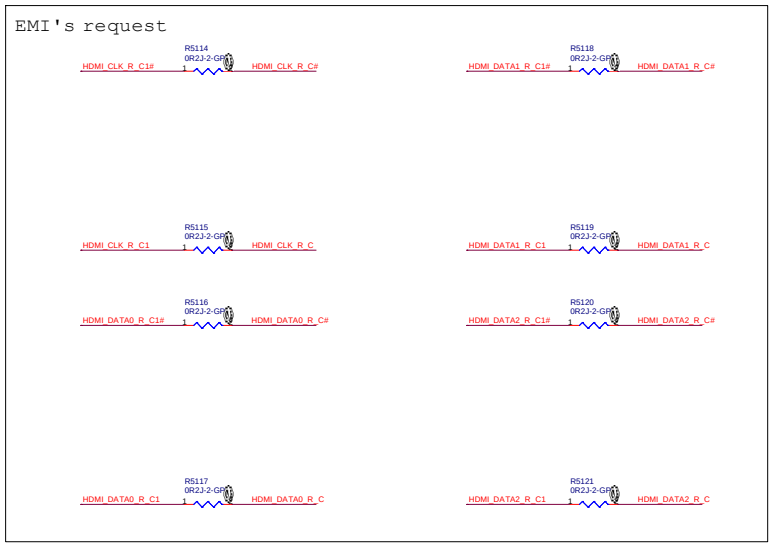
Close to HDMI Connector

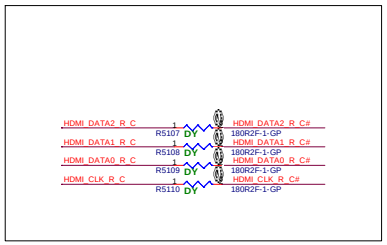


HDMI CONNECTOR

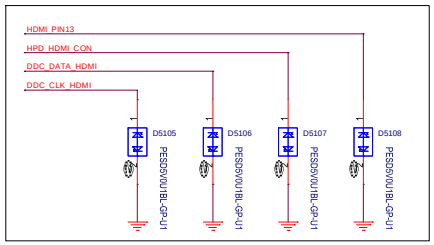


EMI's request

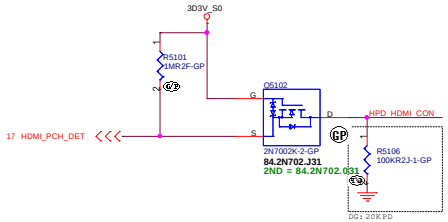


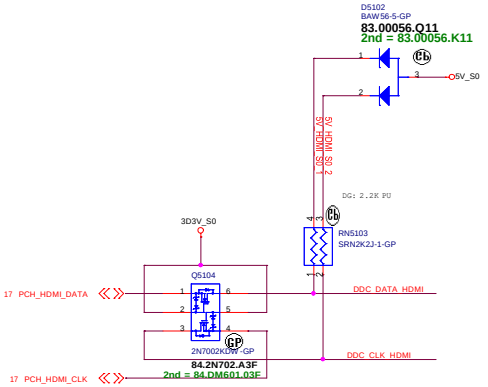


ESD Request



HDMI DDC Passive Level Shifter





<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDMI Level Shifter/Connector

Size: A2 | Document Number: LA480 | Rev: SD

Date: Friday, January 06, 2012 | Sheet 51 of 103

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<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***eDP***

Size	Document Number	Rev
A4	**LA480**	**SD**

Date: Friday, January 06, 2012 Sheet 52 of 103

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<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***S-VIDEO***

Size	Document Number	Rev
A4	**LA480**	**SD**

Date: Friday, January 06, 2012 Sheet 53 of 103

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<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	LA480	SD

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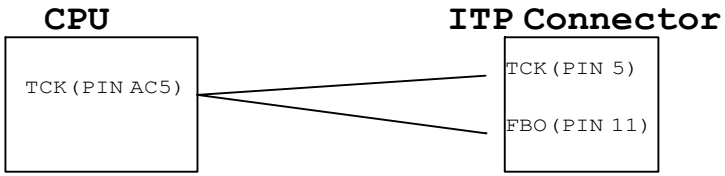
SSID = User.Interface

ITP Connector

H_CPURST# use pull-up Resistor close
ITP connector 500 mil (max),
others place near CPU side.

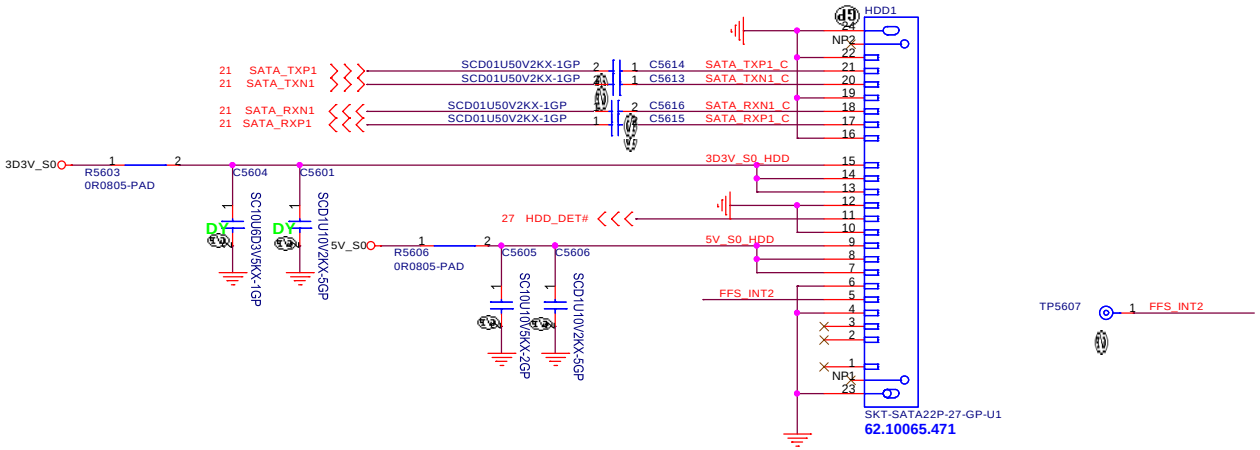


<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ITP		
Size: A4	Document Number: LA480	Rev: SD
Date: Friday, January 06, 2012	Sheet 55 of 103	

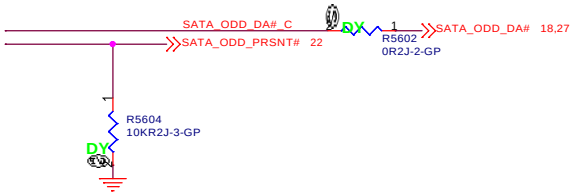
SATA HDD Connector

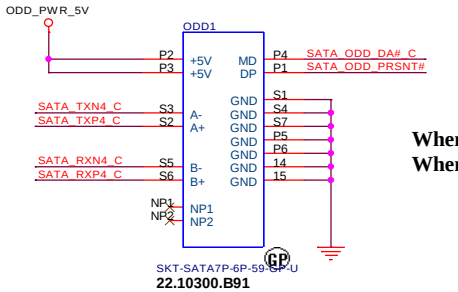


ODD Connector

SATA_RX- and SATA_RX+ Trace Length match within 20 mil

Mars:
Exchange ODD and ESATA differential pair each other.



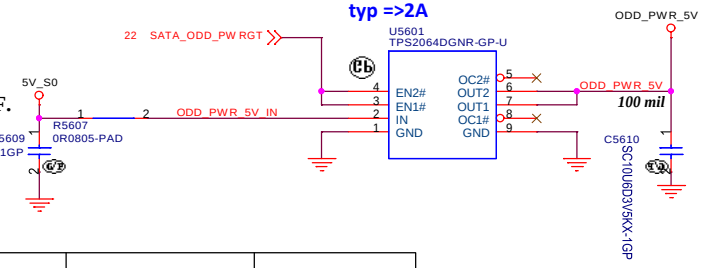


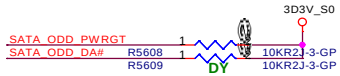
74.02069.079 TI TPS2069DGNR MSOP 8P
74.07534.D79 UPI UP7534PRA8-15 MSOP 8P
74.00547.C79 GMT G547F1P81U MSOP 8P (OBS)
74.07534.A79 UPI UP7534ARA8-15 MSOP8P

When the drive is powered on, the FET to the MD/DA pin drive is OFF.
When the drive is powered off, the FET to the MD/DA pin is ON

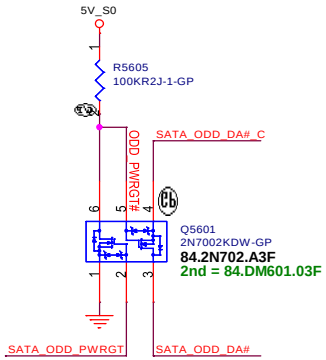
SATA Zero Power ODD

Current limit
Active High
typ =>2A





SUPPORT ZERO SATA ODD



TI	74.02069.079	TPS2069DGNR	High Active
DIODES		AP2171WG-7	High Active
UPI	74.07534.A7F	OBS	High Active

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDD/ODD

Size	Document Number	Rev
A3	LA480	SD

Date: Friday, January 06, 2012 Sheet 56 of 103

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<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***E-SATA+USB***

Size	Document Number	Rev
A4	**LA480**	**SD**

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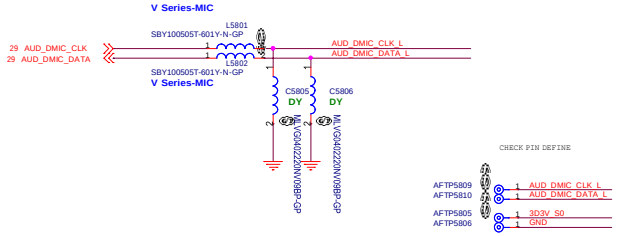
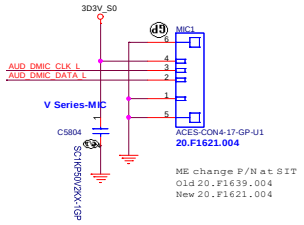
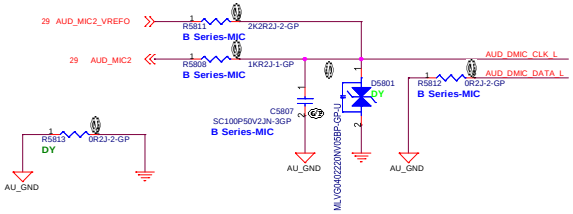
Int. Digital MIC for V series

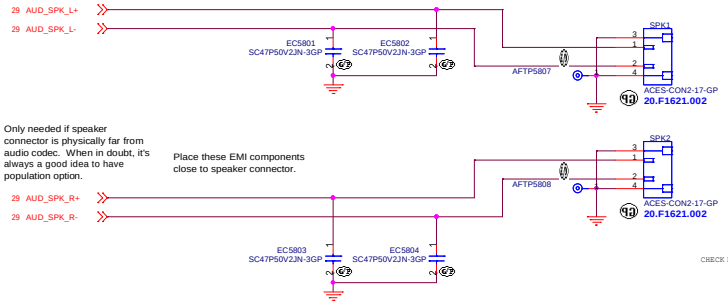




Int. Mono Analog MIC for B series



INTERNAL STEREO SPEAKERS



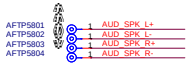


Table 58.1 - Bi-direction ESD multi-source

Supplier	Description	Lenovo P/N	Wistron P/N
ROHM	RSB5.6SMT2R	N/A	83.RSB56.BAF
ON SEMI	ESD5B5.0ST1G	N/A	83.ESD5B.0AF
NXP	PESD5V0S1BB	N/A	83.0005V.0AF

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Audio Jack

Size: A2 | Document Number: LA480 | Rev: SD

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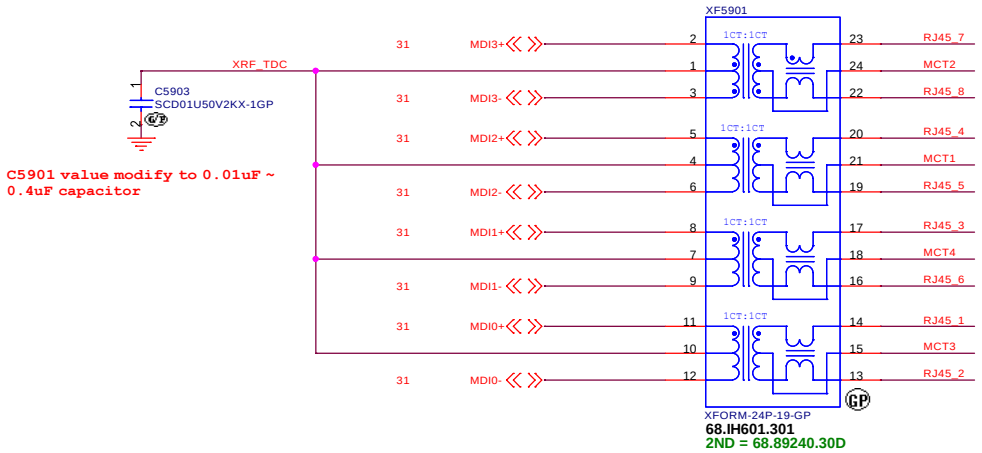
FOR CO-LAY

GIGA Lan Transformer



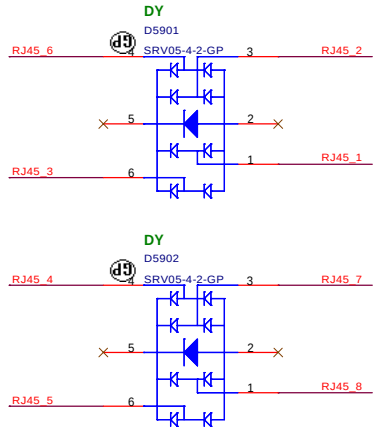
1st
68.IH601.301(Taimag) for 1000
68.HH035.301(Taimag) for 10/100
2nd
68.2413S.30A(Lankom) for 1000
68.H6441.301(Lankom) for 10/100

TVS

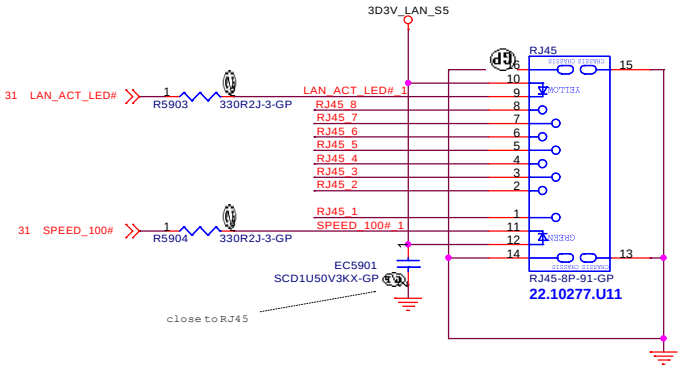
83.00005.BAE
DIODE ARR SRV05-4.TCT SOT-23-6

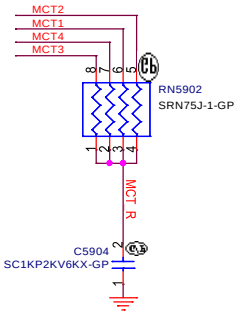
83.09904.AAE
DIODE ESD AZC099-04S SOT23-6L

Swap for V480



LAN Connector





<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

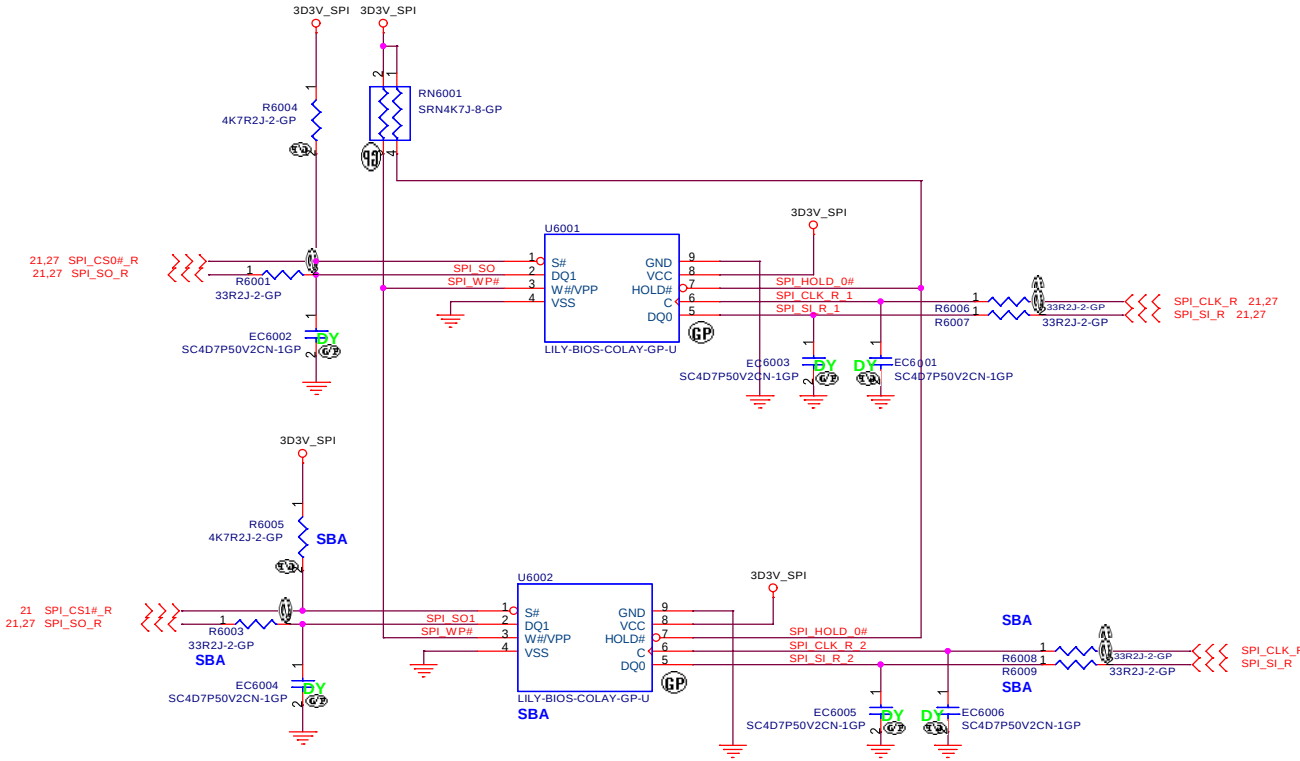
Title: ***RJ45 / Transformer***

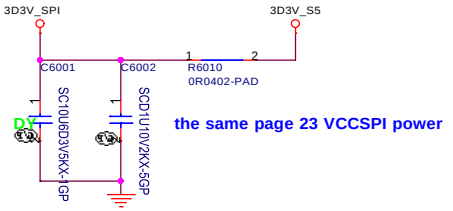
Size	Document Number	Rev
A3	LA480	SD

Date: Friday, January 06, 2012 Sheet 59 of 103

SSID = Flash.ROM

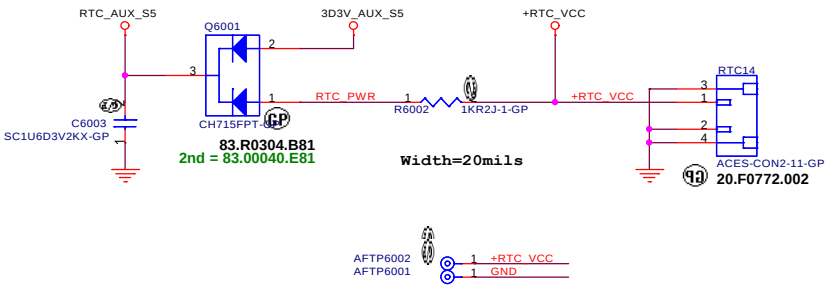
SPI FLASH ROM (8M byte) for PCH

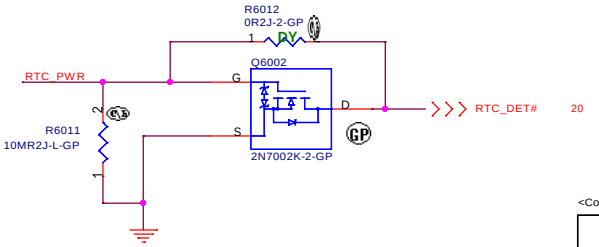




4MB			
SO8	Marcronix	MX25L3206EM2I-12G	72.25320.C01
	Winbond	W25Q032BVSSIG	72.25Q32.A01
	Numonyx	N25Q032A13ESE40	72.25032.H01
8MB			
SO8	Marcronix	MX25L6406EM2I-12G	72.25640.D01
	Winbond	W25Q064CVSSIG	72.25Q64.B01
	Numonyx	N25Q064A13ESE40	72.25Q64.D01
16MB			
WSON	Marcronix	MX25L12836EZNI-10G	72.25128.X01
		MX25L12835EZNI-10G	72.25128.Y01
	Winbond	W25Q128BVEIG	72.25128.I01
	Numonyx	N25Q128A13EF840	72.25128.B03

SSID = RBATT





<Core Design>

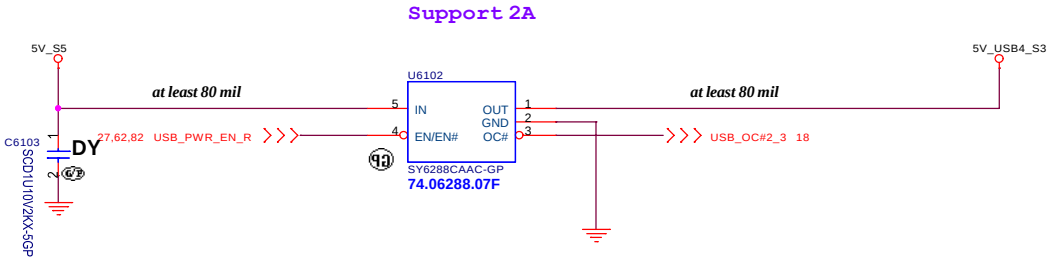
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Flash/RTC

Size	Document Number	Rev
A3	LA480	SD

Date: Friday, January 06, 2012 Sheet 60 of 103

USB Board CONN.



Place U6102 close to USBCN1

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***USB Connector***

Size	Document Number	Rev
A3	LA480	SD

Date: Friday, January 06, 2012 Sheet 61 of 103

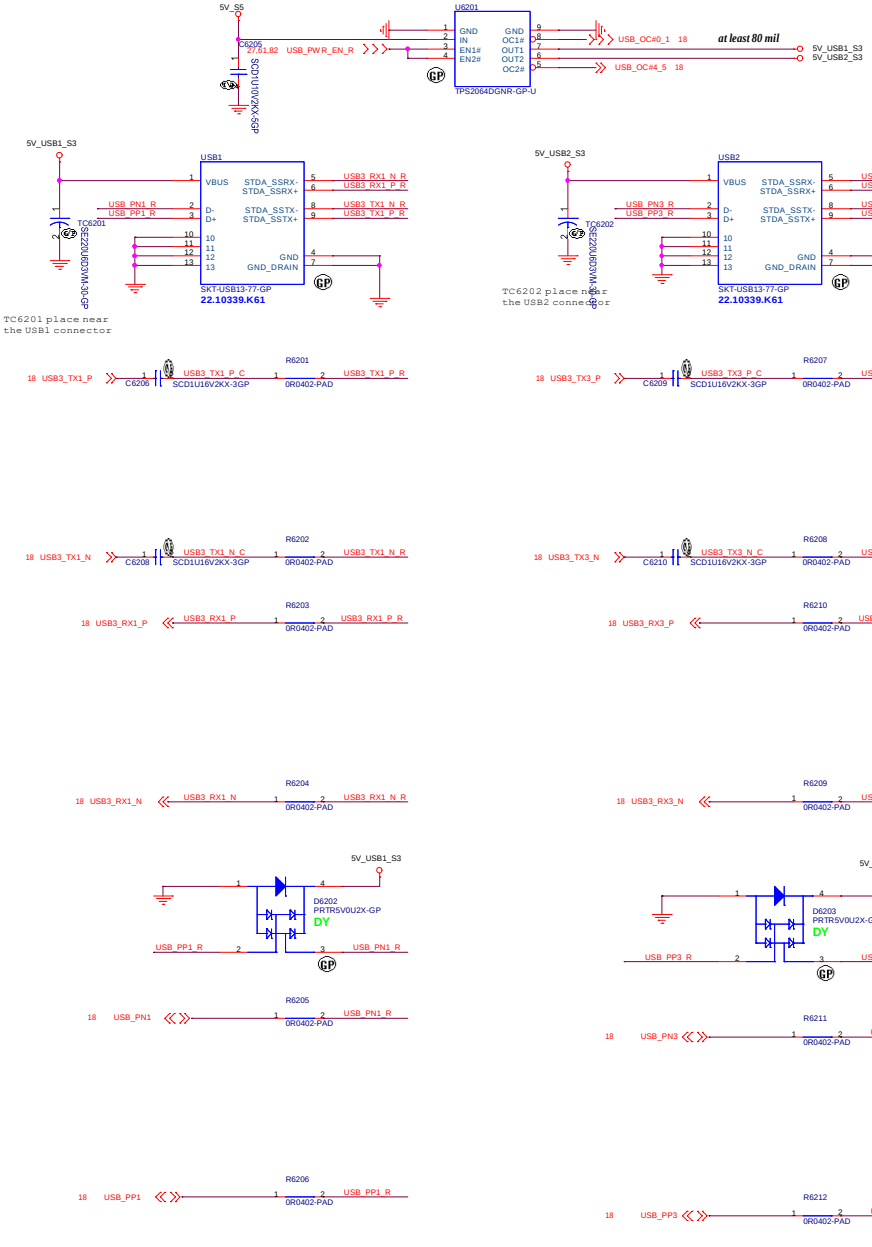
USB3.0 Port1

USB3.0 Port2

USB3.0 Port3

USB3.0 Port4

2A



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

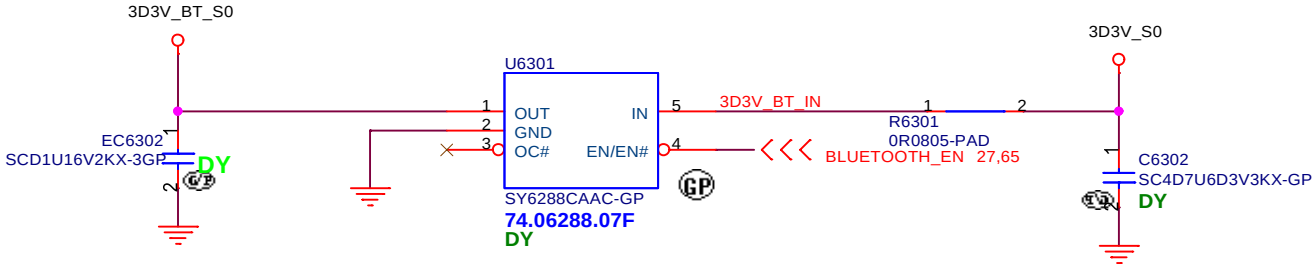
Title: *USB 3.0 Port*2*

Size: A2 | Document Number: LA480 | Rev: SD

Date: Friday, January 06, 2012 | Sheet 62 of 103

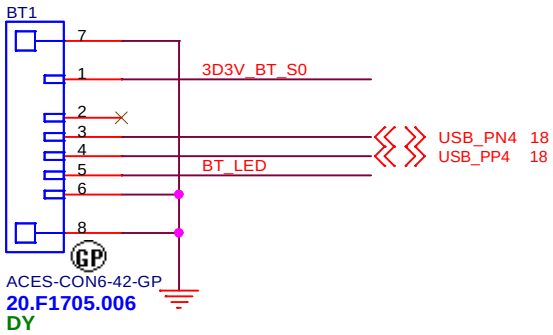
SSID = User.Interface

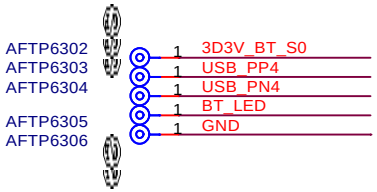
Bluetooth conn.



SILERGY	74.06288.07F	SY6288CAAC	High Active
DIODES	74.02171.07F	AP2171WG-7	High Active
UPI	74.07534.A7F	OBS	High Active
GMT	74.05240.A7F	OBS	High Active

BT Module pin definition is same as LA470





<Core Design>

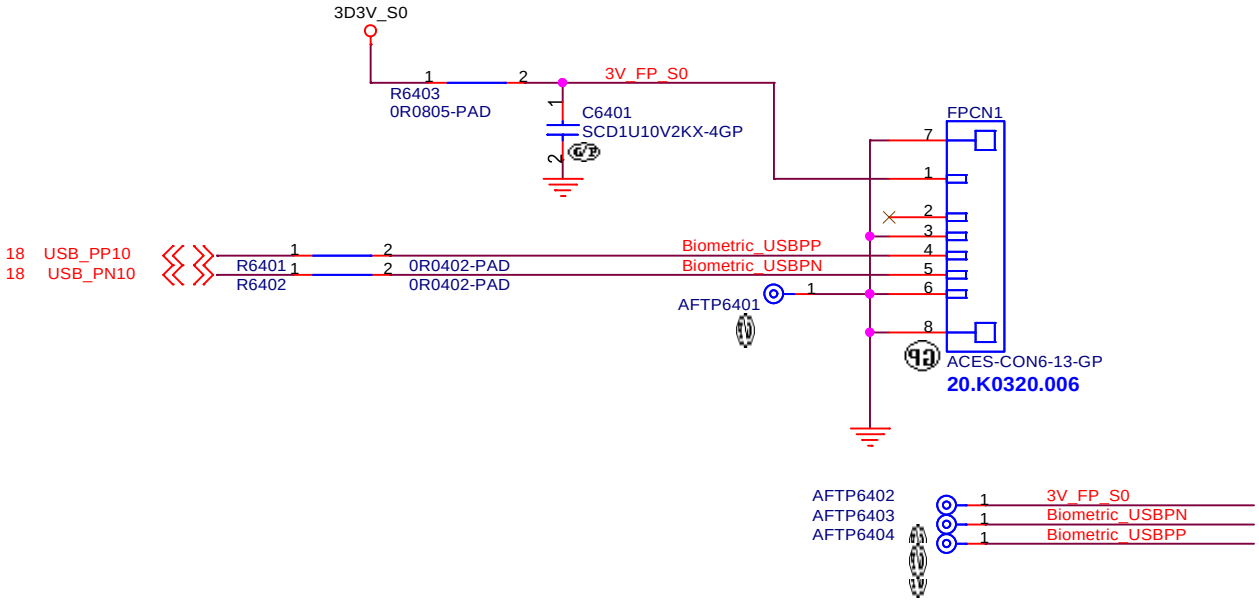
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Bluetooth***

Size	Document Number	Rev
A4	LA480	SD

Date: Friday, January 06, 2012 Sheet 63 of 103

Finger Printer Connector



<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

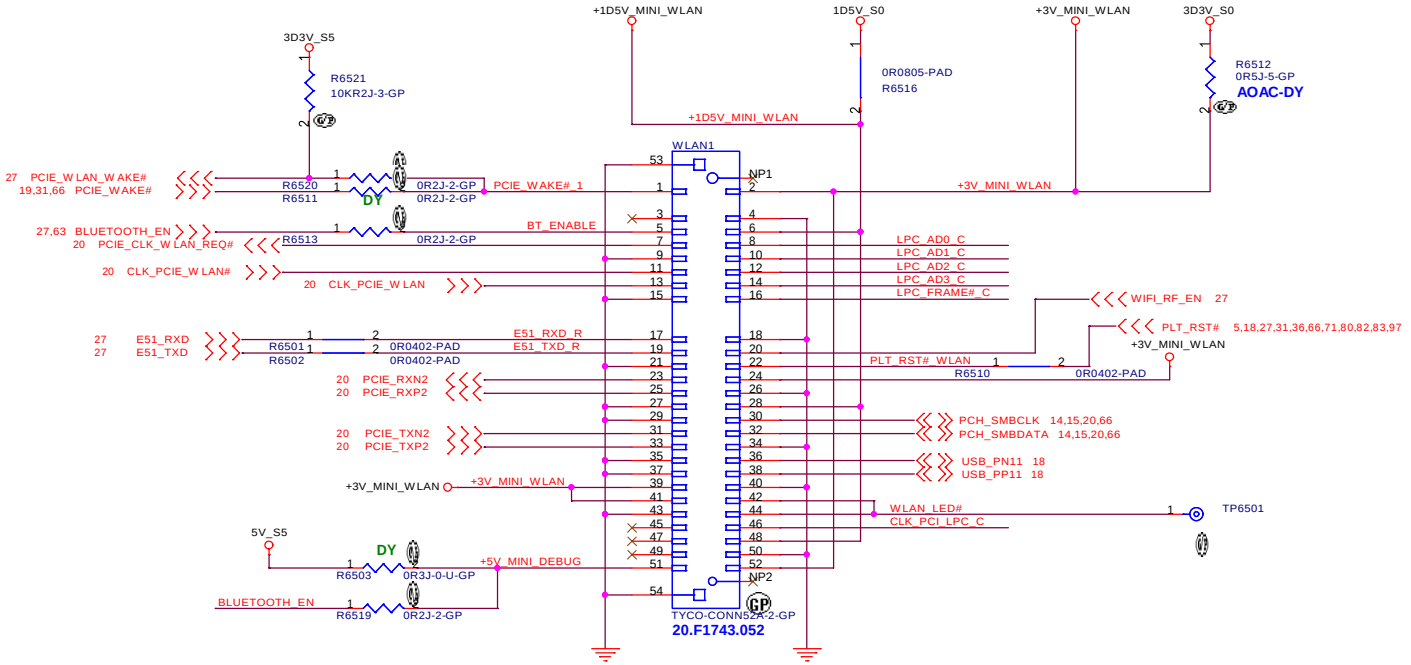
Title: ***Finger Printer Connector***

Size	Document Number	Rev
A4	LA480	SD

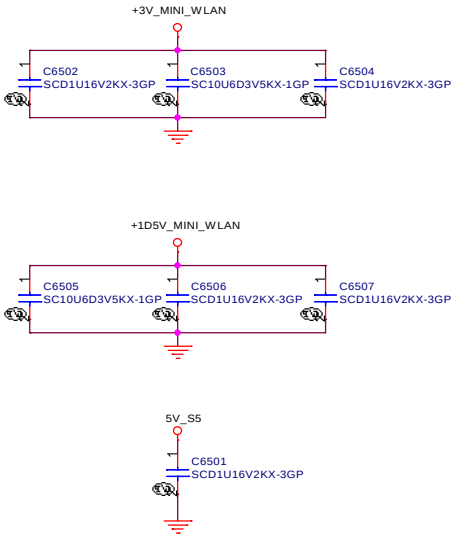
Date: Friday, January 06, 2012 Sheet 64 of 103

SSID = Wireless

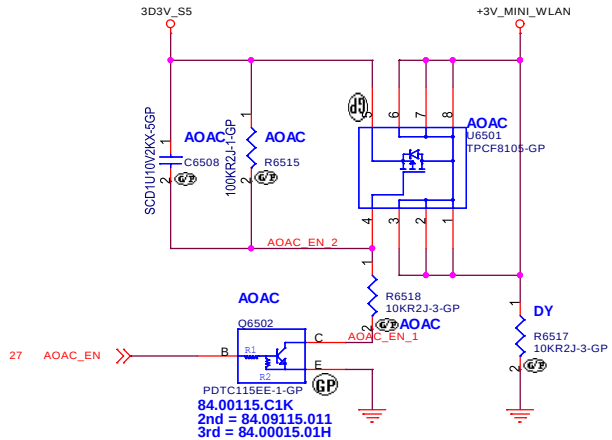
Mini Card Connector(802.11a/b/g/n)

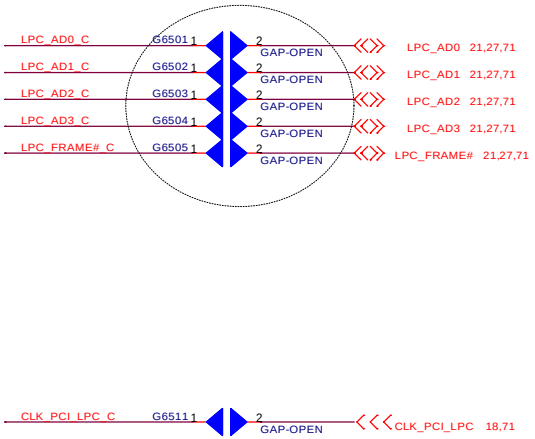


Place near MINI Card CONN



Reserve for AOAC





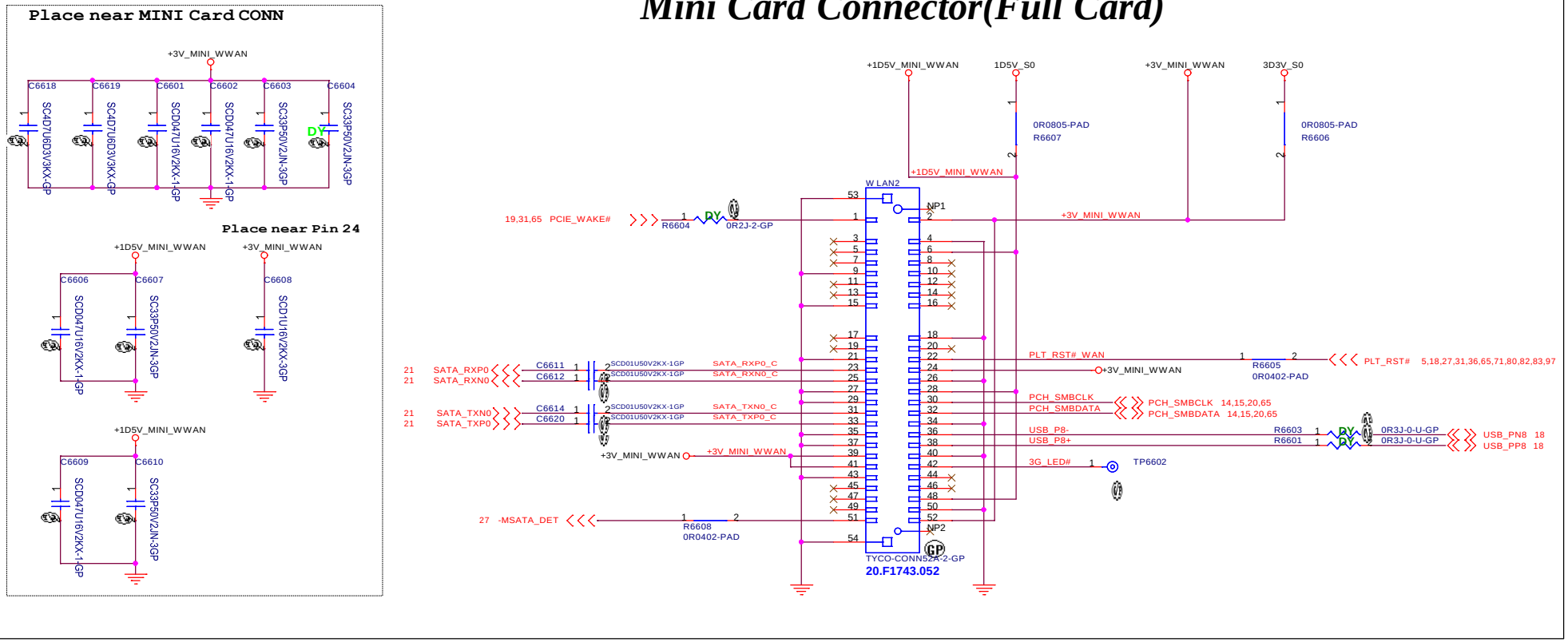
G6506~G6511 placememt close close WLAN1 in bottom side

<Core Design>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *MINICARD(WLAN)/ITP CONN*		
Size: A3	Document Number: LA480	Rev: SD
Date: Friday, January 06, 2012	Sheet 65 of 103	

SSID = Wireless

mSATA for V Series Only



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***WWAN Connector***

Size	Document Number	Rev
A3	LA480	SD

Date: Friday, January 06, 2012 Sheet 66 of 103

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<Core Design>

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

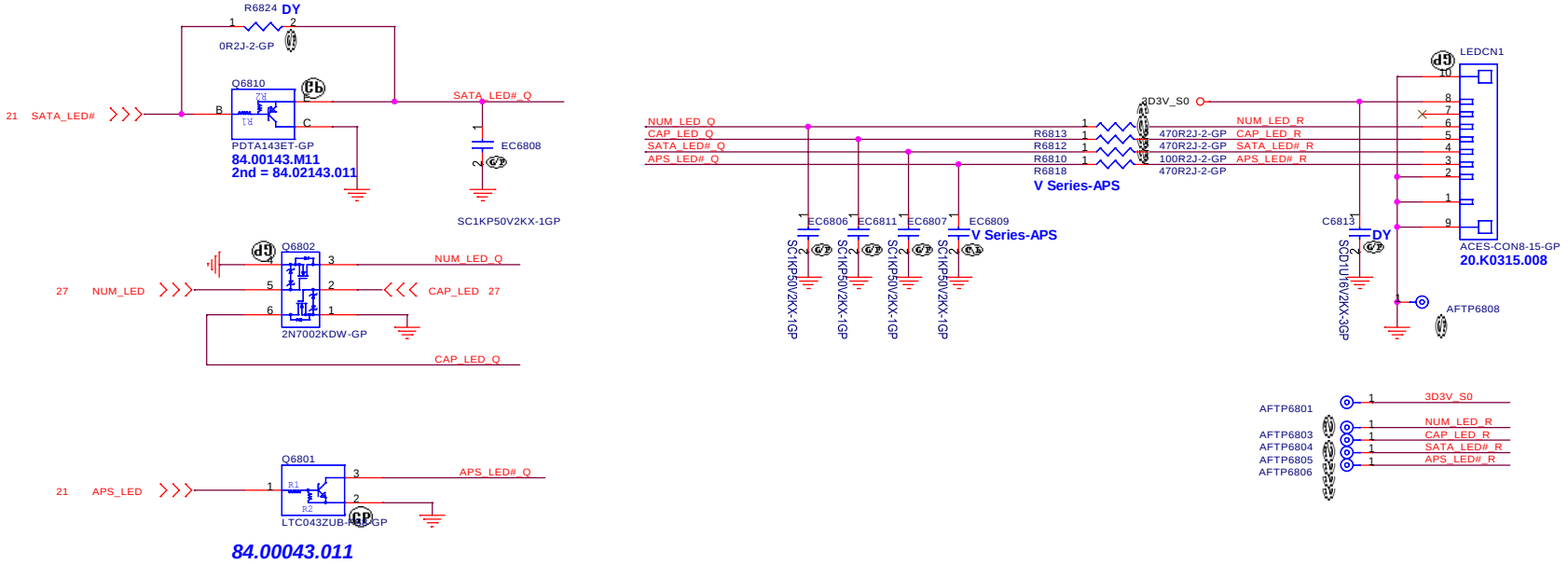
Title

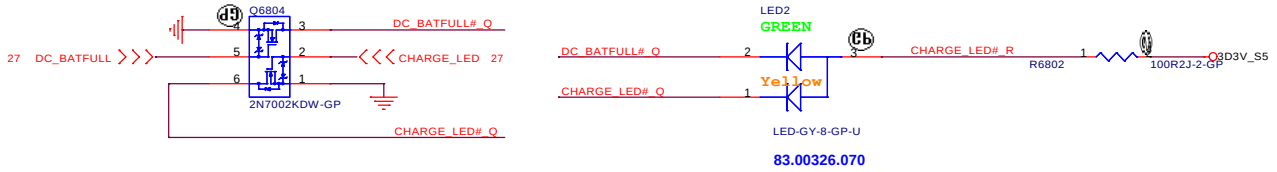
Reserved

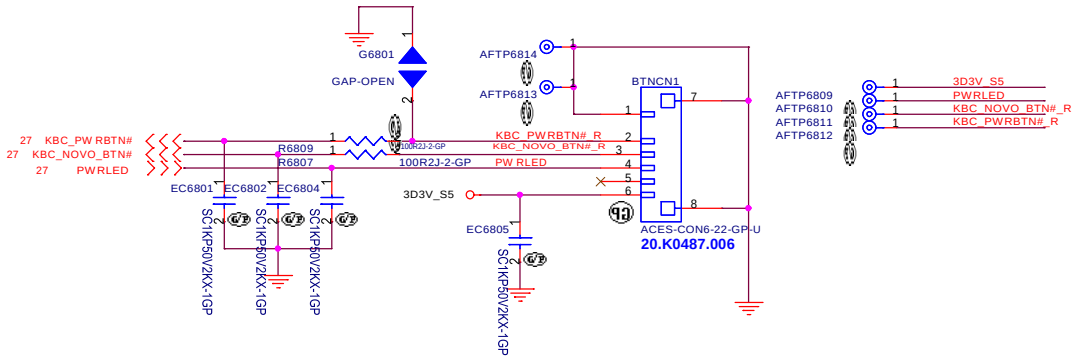
Size	Document Number	Rev
A4	**LA480**	**SD**

Date: Friday, January 06, 2012 Sheet 67 of 103

SSID = User.Interface







<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

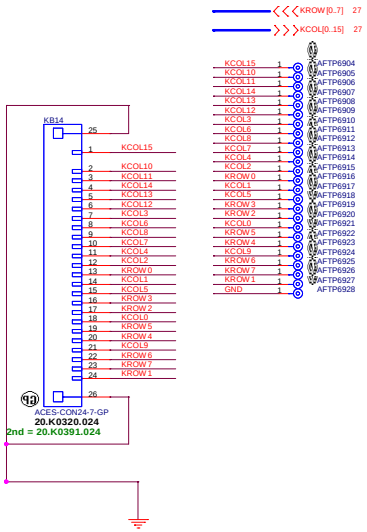
Title: *LED Bard/Power Button*

Size	Document Number	Rev
A3	LA480	SD

Date: Friday, January 06, 2012 Sheet 68 of 103

SSID = KBC

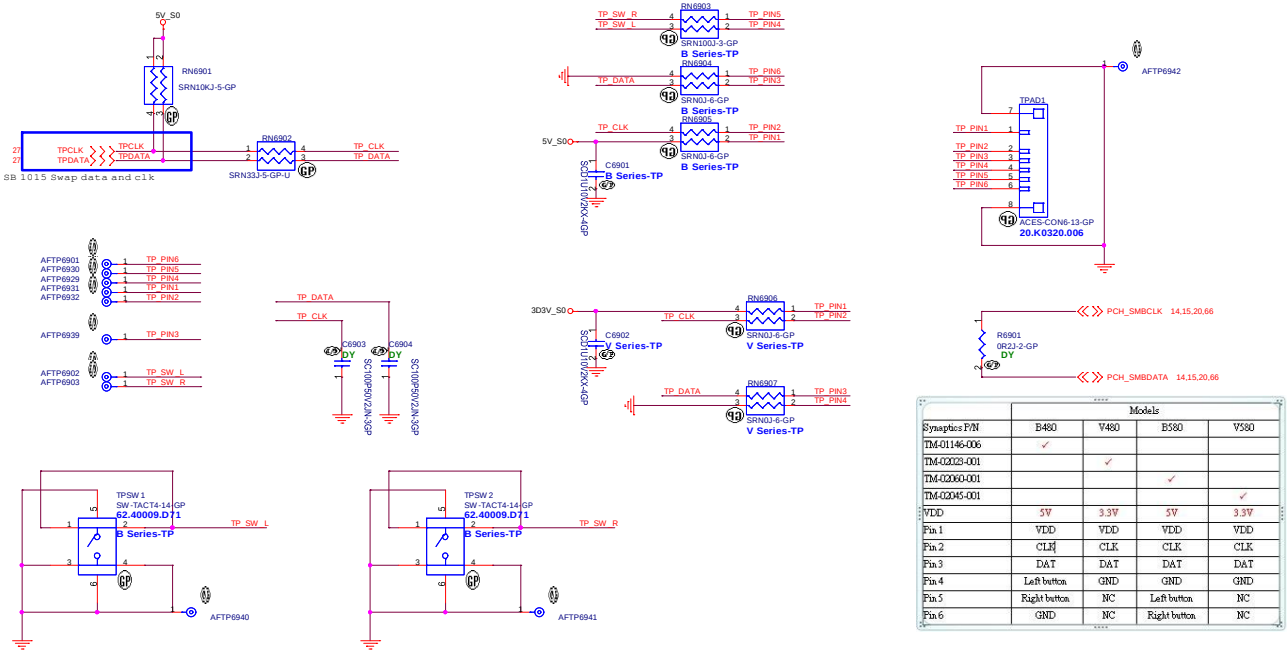
Internal KeyBoard Connector



KB14 for 14" VB480 & VB485
KB15 for 15" VB580 & VB585

SSID = Touch.Pad

Normal Pad for B Series 5V
ClickPad for V Series 3.3V



Synaptics P/N	Models			
	B480	V480	B580	V580
TM-01146-006	✓			
TM-02023-001		✓		
TM-02060-001			✓	
TM-02045-001				✓
VDD	5V	3.3V	5V	3.3V
Pin 1	VDD	VDD	VDD	VDD
Pin 2	CLK	CLK	CLK	CLK
Pin 3	DAT	DAT	DAT	DAT
Pin 4	Left button	GND	GND	GND
Pin 5	Right button	NC	Left button	NC
Pin 6	GND	NC	Right button	NC

* Membrane Pin Out Top View :

PIN #	7	11	13	18	14	10	17	15	16	4	23	22	19	20	21	24	12	1	8	9	5	6	3	2
As-sign	D 1	D 2	D 3	D 4	D 5	D 6	D 7	D 8	D 9	D 10	D 11	D 12	D 13	D 14	D 15	D 16	S 1	S 2	S 3	S 4	S 5	S 6	S 7	S 8

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **TOUCH PAD CONNECTOR**

Size: A2 | Document Number: **LA480** | Rev: **SD**

Date: Friday, January 06, 2012 | Sheet 69 of 103

<Core Design>

緯創資通

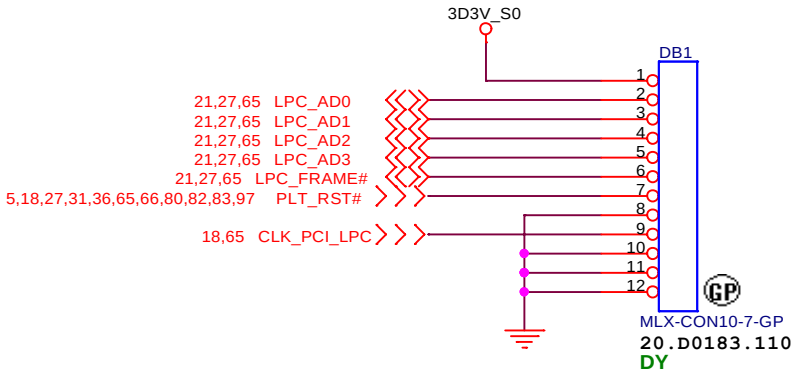
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Hall Sensor

Size	Document Number	Rev
A4	**LA480**	**SD**

Date: Friday, January 06, 2012 Sheet 70 of 103



<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Dubug connector***

Size	Document Number	Rev
A4	**LA480**	**SD**

Date: Friday, January 06, 2012 Sheet 71 of 103

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<Core Design>

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size	Document Number	Rev
A4	**LA480**	**SD**

Date: Friday, January 06, 2012 Sheet 72 of 103

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<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	**LA480**	**SD**

Date: Friday, January 06, 2012 Sheet 73 of 103

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai W u Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***CARD Reader CONN***

Size	Document Number	Rev
A2	**LA480**	**SD**

Date: Friday, January 06, 2012 Sheet 74 of 103

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<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***New Card***

Size	Document Number	Rev
A4	**LA480**	**SD**

Date: Friday, January 06, 2012 Sheet 75 of 103

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<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	**LA480**	**SD**

Date: Friday, January 06, 2012 Sheet 76 of 103

<Core Design>

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size	Document Number	Rev
A4	**LA480**	**SD**

Date: Friday, January 06, 2012 Sheet 77 of 103

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<Core Design>

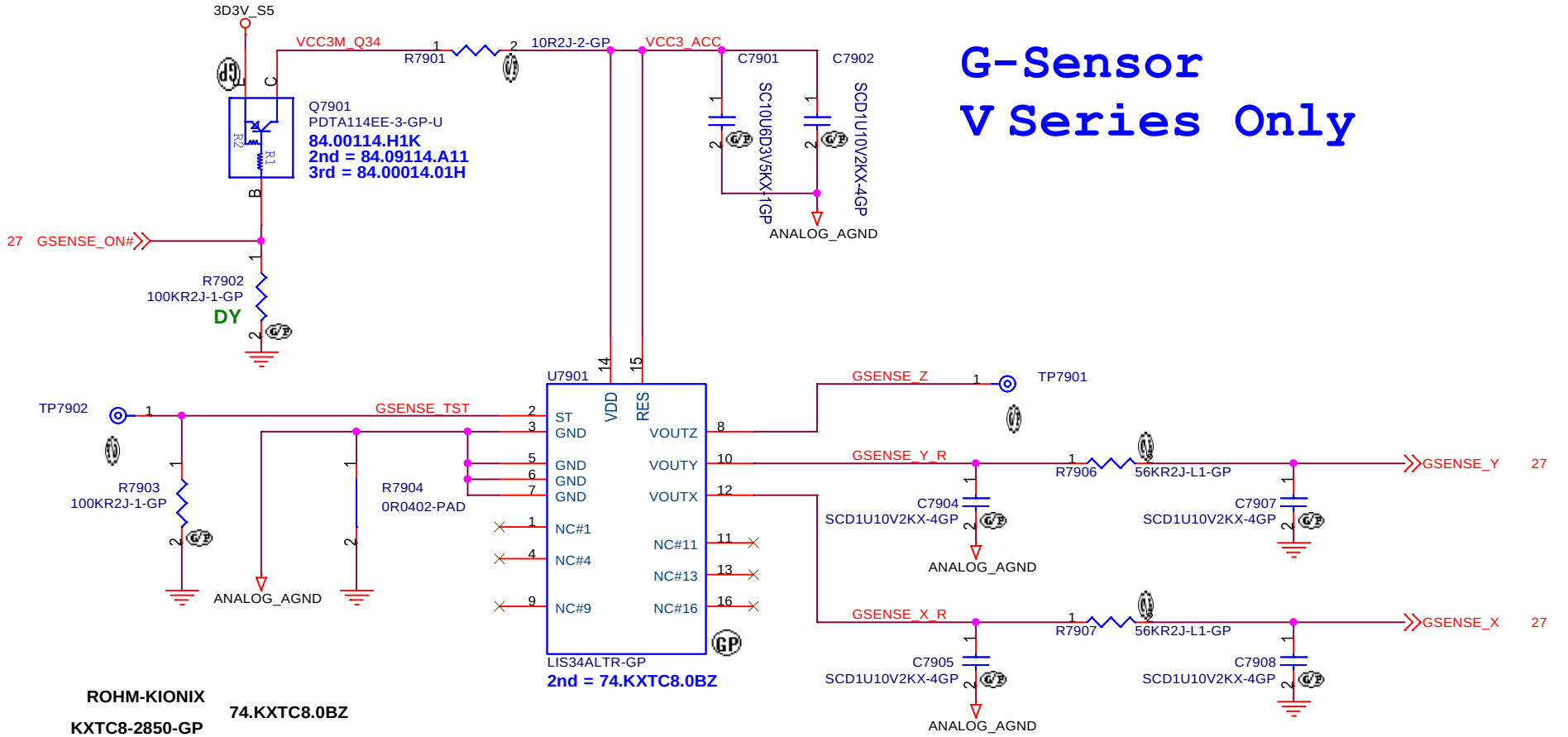
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	**LA480**	**SD**

Date: Friday, January 06, 2012 Sheet 78 of 103

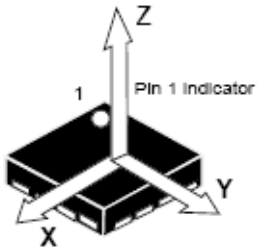
G-Sensor
V Series Only



ROHM-KIONIX

KXTC8-2850-GP

74.KXTC8.0BZ



Layout Comment :

(1) Place C483, C484, Q46, R528, R530, C479, C476, R509, R508 close to U55.

(2) Avoid routing under DCDC switching area.

<Core Design>

緯創資通 **Wistron Corporation**

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: **G-Sensor**		
Size: A4	Document Number: **LA480**	Rev: **SD**
Date: Friday, January 06, 2012	Sheet 79 of 103	

RFID

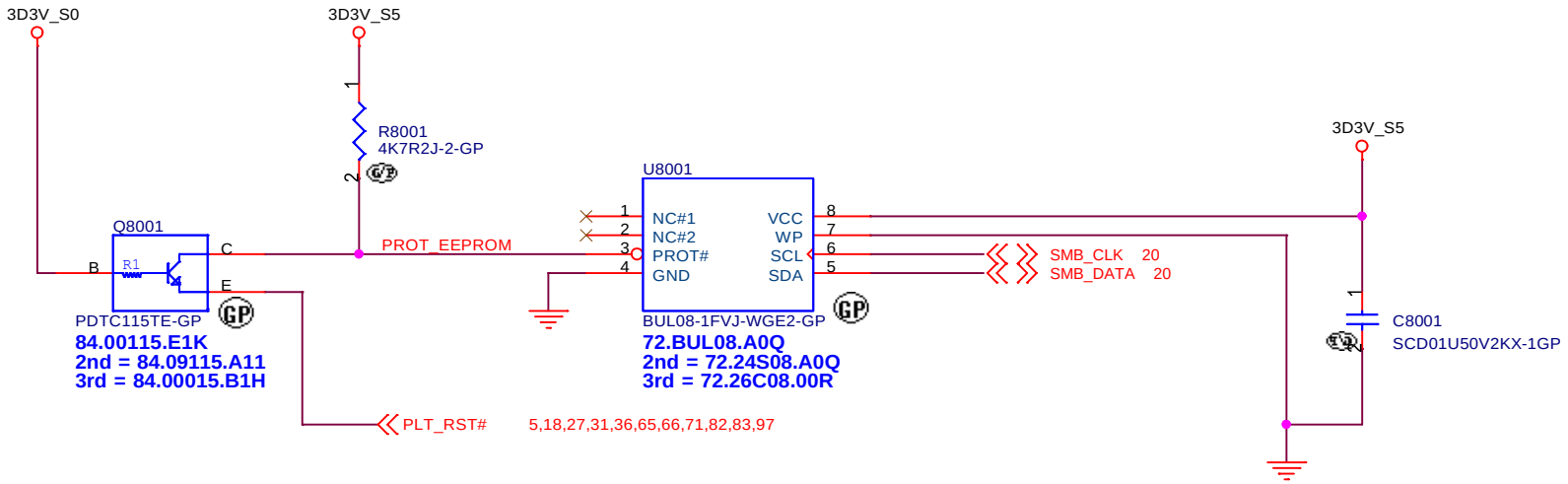

Table 80.1- Transistor multi-source

Supplier	Description	Lenovo P/N	Wistron P/N
NXP	PDTC115TE	N/A	84.00115.E1K
ROHM	LTC015TEB	N/A	84.00015.B1H
Panasonic	DRC9115T0L	N/A	84.09115.A11

Table 80.2- EEPROM multi-source

Supplier	Description	Lenovo P/N	Wistron P/N
ROHM	BUL08-1FVJ-WGE2	N/A	72.BUL08.A0Q
NXP	PCA24S08ADP	N/A	72.24S08.A0Q
SANYO	LE26CAP08TT-TLM-H	N/A	72.26C08.00R

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **RF ID**

Size: A4 | Document Number: **LA480** | Rev: **SD**

Date: Friday, January 06, 2012 | Sheet 80 of 103

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<Core Design>

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

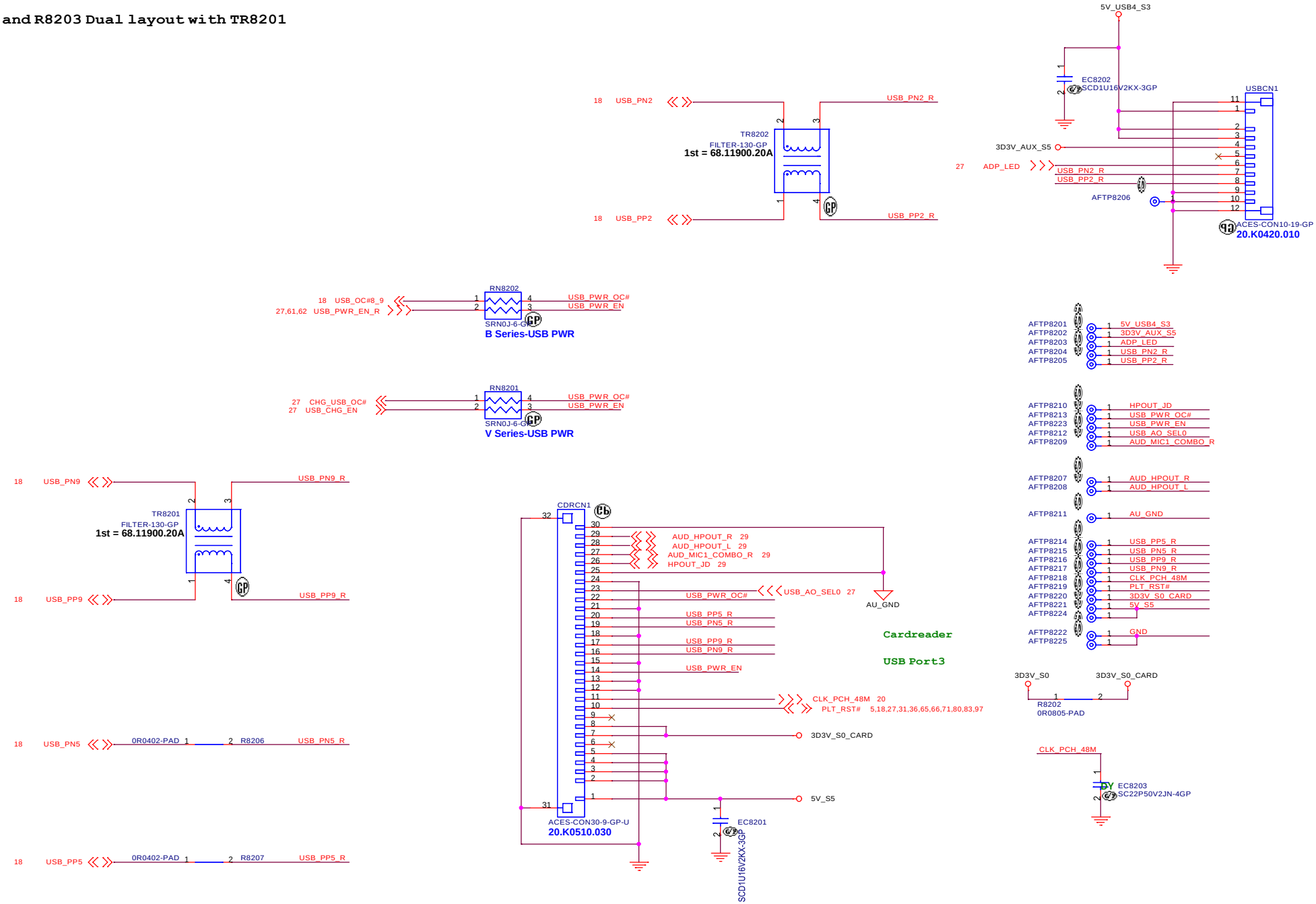
Title

Reserved

Size	Document Number	Rev
A4	**LA480**	**SD**

Date: Friday, January 06, 2012 Sheet 81 of 103

R8201 and R8203 Dual layout with TR8201



<Core Design>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***IO Board Connector***	
Size A3	Document Number **LA480**	Rev **SD**
Date: Friday, January 06, 2012	Sheet 82 of 103	

SPEC. (DG-05587-001_v03_p.70)
PEX_CLK_REQ_N is an open-drain bi-directional signal;
by default it should have a 10 kΩ pull-up to 3.3V.
This signal is an active low signal.

PCI Express PEX_IOVVD/Q Combined (DG-05587-001_v03_p.72_Table 10)

Capacitor	Type	Footprint	Population	Location
1.0uF	X6S	0402	4	Under GPU
4.7uF	X6S	0603	2	Near GPU
10uF	X5R	0805	4	Midway Between GPU and Power Supply
22uF	X5R	0805	4	Midway Between GPU and Power Supply

X6S (+/-22%, -55~105°C
X5R (+/-15%, -55~85°C

1.05V ±30mV 3300mA total
(DG-05587-001_v03_p.71_Table 9)

1uF(X5R) K0402 ×4
4.7uF(X5R) K0603 ×2
10uF(X5R) M0805 ×4
22uF(X5R) M0805 ×4

Under GPU
Near GPU
Midway Between GPU and Power Supply

SPEC. (DG-05587-001_v03_p.70)
For PCI ECPRESS connection,
please use 0.22uF,20%,0402,X5R
or better AC coupling capacitors.

0.22uF(X5R) K0402

PCI Express PEX_SVDD/PLL_HVDD Connected to NV3V3 (DG-05587-001_v03_p.72_Table 12)

Capacitor	Type	Footprint	Population	Location
0.1uF	X5R	0402	1	Near GPU
4.7uF	X5R	0603	2	Near GPU

X5R (+/-15%, -55~85°C

3.3V ±10% 210mA total
(DG-05587-001_v03_p.71_Table 9)

0.1uF(X5R) K0402 ×1
4.7uF(X5R) K0603 ×2

Near GPU

dGPU reset

SPEC. (DG-05587-001_v03_p.70)
PEX_TSTCLK_OUT should be
terminated with a 200Ω resistor.

PCI Express PEX_PLLVDD (DG-05587-001_v03_p.72_Table 11)

Capacitor	Type	Footprint	Population	Location
100nF	X6S	0402	1	Under GPU
1.0uF	X5R	0603	1	Near GPU
4.7uF	X5R	0805	1	Near GPU

X6S (+/-22%, -55~105°C
X5R (+/-15%, -55~85°C

100nF(X7R) K0402 ×1
1.0nF(X5R) K0402 ×1
4.7nF(X5R) K0603 ×1

1.05V ±30mV 150mA total
(DG-05587-001_v03_p.71_Table 9)

Under GPU
Near GPU

Stuff 0 ohm(63.00000.00L) for N13P-GS/N13M-GS,
Stuff bead(68.00082.001) for N13P-GL/N13M-GE

SPEC. (DG-05587-001_v03_p.214)
By default, pull-down the TESTMODE pin to GND with a 10kΩ resistor.
For XOR tree testing, TESTMODE should be pulled up to 3v3 with a 10 kΩ resistor.

SPEC. (DG-05587-001_v03_p.70)
PEX_TERMP is used for internal calibration;
pull-down this signal with 2.49 kΩ,1% resistor.

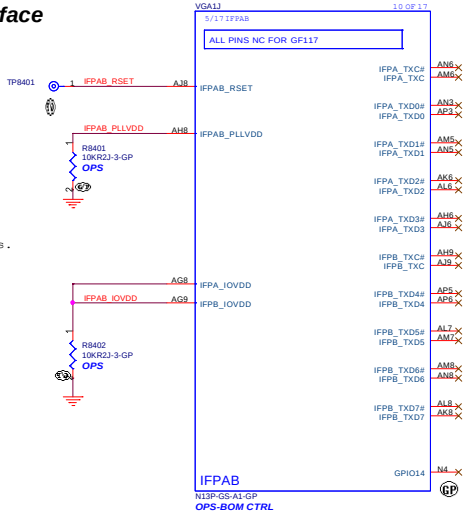
<Core Design>

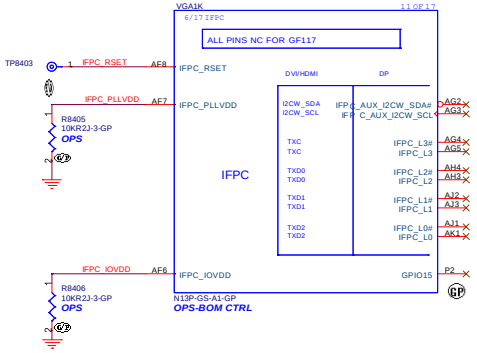
Wistron Corporation
21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih,
Taipei Hsien 221, Taiwan, R.O.C

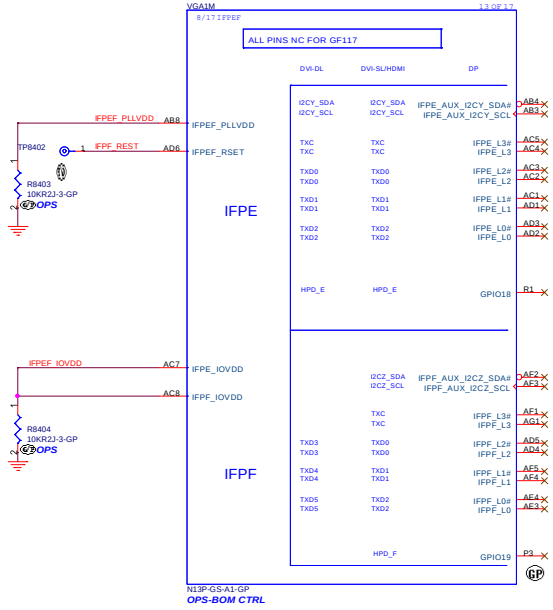
Title: N13P_GPU (1/5): PEG
Size: A2
Document Number: LA48
Rev: SD
Date: Friday, January 06, 2012
Sheet 83 of 103

LVDS Interface

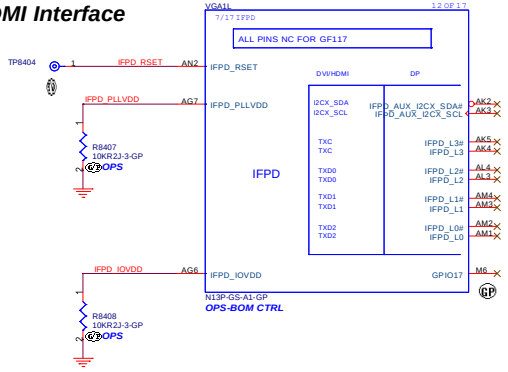
SPEC. (DG-05587-001_v03_p.160)
Pull down IFPxy IOVDD with 10kΩ resistor.
Pull down IFPxy PLLVDD with 10kΩ resistor.
The other IO pins can be NC, this includes unused data lines.







HDMI Interface



<Core Design>

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Title	N13P_GPU (2/5): DIGITALOUT
Size: A2	Document Number: LA48
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Date: Friday, January 06, 2012	Sheet 84 of 103

E1 (DA-05691-001_v03_04 Table 2)
N13P-GL NC
N13M_GE1 NC
N13M-GS Pull down FB_CLAMP with a 10kΩ
N13P-GS Pull down FB_CLAMP with a 10kΩ

35mA
(DG-05587-001_v03_p.88_Table 25)

Mode D Command Mapping
(DG-05587-001_v03_p.78_Table 16)

N13x DDR3 mode D	Data Bits [31:0]	Data Bits [63:32]
FBx_CMD0	CS0#	
FBx_CMD1		
FBx_CMD2	ODT	
FBx_CMD3	CKE	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#
FBx_CMD17		
FBx_CMD18		ODT
FBx_CMD19		CKE
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#
FBx_CMD31		

FB CMD mapping
Mode D-N13x

FB CMD mapping
Mode D-N13x

66mA
(DG-05587-001_v03_p.88_Table 25)

1.05V ±30mV 167mA total
100nF(X7R)
K0402 ×3

66mA
(DG-05587-001_v03_p.88_Table 25)

Stuff 0 ohm(63.00000.00L) for N13P-GS/N13M-GS,
Stuff bead(68.00084.H41) for N13P-GL/N13M-GE

Under GPU

GPU FBVDDQ Decoupling (DG-05587-001_v03_p.86_Table 22)

Capacitor	Type	Footprint	Population	Location
0.1uF	X7R	0402	8	Under GPU
1uF	X7R	0603	2	Under GPU
4.7uF	X6S	0603	2	Under GPU
10uF	X5R	0805	4	Near GPU

X7R (+/-15%, -55~125°C)
X6S (+/-22%, -55~105°C)
X5R (+/-15%, -55~85°C)

0.1uF(X7R)
K0402 ×8

Under GPU

1uF(X7R)
K0603 ×4

Near GPU

4.7uF(X5R)
K0603 ×2

10uF(X5R)
M0805 ×2

Default GPU Drive Calibration for DDR3 (DG-05587-001_v03_p.82_Table 17)

Memory/PKG	FBVDDQ	FBCAL_PU_GND	FBCAL_PU_VDDQ	FBCAL_TERM_GND
DDR3	1.5V	42.2Ω	40.2Ω	51.1Ω

*Use only 1% resistors for driver calibration.

FBx_PLL_AVDD, FB_DLL_AVDD and PLLVDD combined
(DG-05587-001_v03_p.88_Table 26)

Capacitor	Type	Footprint	Population	Location
100nF 22uF	X7R X5R	0402 0805	1 per pin 1	Under GPU Near GPU
Bead Type				
30Ω @100MHz (ESR=0.01Ω)		0603	1	Near GPU

X7R (+/-15%, -55~125°C)
X5R (+/-15%, -55~85°C)

Memory ODTx, CKEx and RST Termination
(DG-05587-001_v03_p.84_Table 20)

FBCLK Termination placed at each VRAM
(DG-05587-001_v03_p.83_Table 19)

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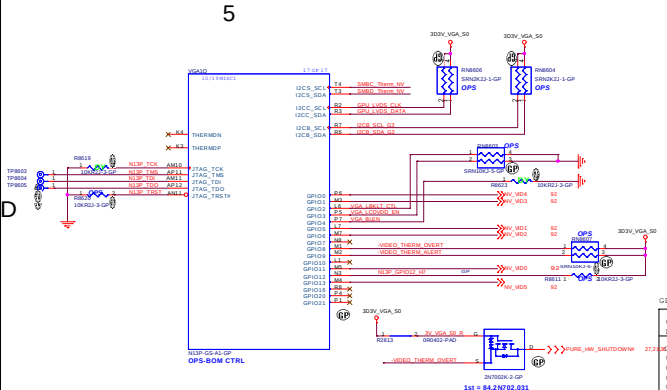
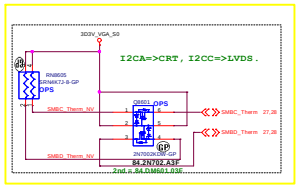
Taipei Hsien 221, Taiwan, R.O.C

Title: N13P_GPU (3/5): VRAM I/F

Size: A2 | Document Number: LA48 | Rev: SD

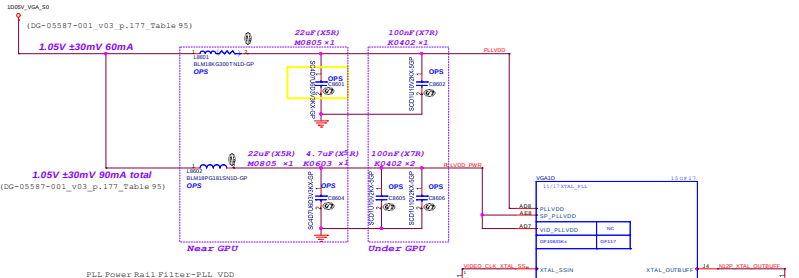
Date: Friday, January 06, 2012 | Sheet 85 of 103





GPIO Description (DG-05587-001_v03_p.82_Tale 98)

GPIO pin Name	Normal Function	I/O	Function Description
GPIO0	GPU_VID4	O	GPU Core VDD VID4
GPIO1	GPU_VID3	O	GPU Core VDD VID3
GPIO2	LCD_BL_PWM	O	Panel Backlight PWM Brightness Control
GPIO3	LCD_VCC	O	Panel Power Enable
GPIO4	LCD_BLEN	O	panel Backlight Enale
GPIO5	GPU_VID1	O	GPU Core VDD VID1
GPIO6	GPU_VID2	O	GPU Core VDD VID2
GPIO7	3D Vision	O	3D Vision Left/Right signal
GPIO8	OVERT	I/O	Active Low Thermal Catastrophic Over Temperature
GPIO9	ALERT	I/O	Active Low Thermal Alert
GPIO10	MEM_VREF_CTL	O	Memory VREF Control
GPIO11	GPU_VID0	O	GPU Core VDD VID0
GPIO12	PWR_LEVEL	I	AC Power Detect Input. High = AC, Low = Battery
GPIO13	GPU_VID5	O	GPU Core VDD VID5
GPIO14	HPD_AB	I	Hot Plog Detect for IFPAB
GPIO15	HPD_C	I	Hot Plog Detect for IFPC
GPIO16	MEM_VDD_CTL	O	Memory VDD VID
GPIO17	HPD_D	I	Hot Plog Detect for IFPD
GPIO18	HPD_E	I	Hot Plog Detect for IFPE
GPIO19	HPD_F	I	Hot Plog Detect for IFPF
GPIO20	Reserved		
GPIO21	Reserved		



PLL Power Rail Filter-PLL_VDD
(DG-05587-001_v03_p.177_Table 96)

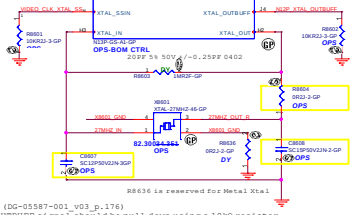
Capacitor	Type	Footprint	Population	Location
100nF	X7R	0402	1	Under GPU
22uF	X7R	0805	1	Near GPU
Bead Type				
30Ω(ESR=0.05)		0402	1	Near GPU

X7R (+/-15%、-55~125°C

PLL Power Rail Filter-SP_PLLVDD and VIDPLLVDD Combined
(DG-05587-001_v03_p.178_Table 97)

Capacitor	Type	Footprint	Population	Location
100nF	X7R	0402	2	Under GPU
4.7uF	X7R	0402	1	Near GPU
22uF	X7R	0805	1	Near GPU
Bead Type				
180Ω(ESR=0.2)		0603	1	Near GPU

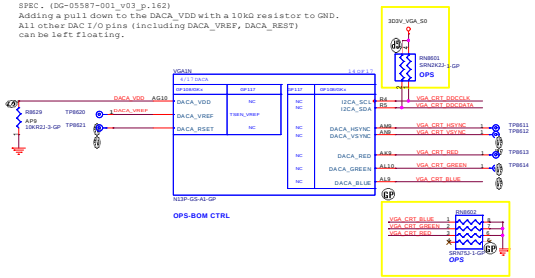
X7R (+/-15%、-55~125°C

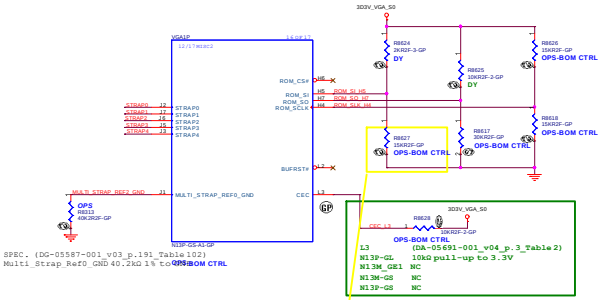


SPEC. (DG-05587-001_v03_p.176)
XTALOUTBUFF signal should be pull down using a 10KΩ resistor.
XTALSSIN signal should be pull down using a 10KΩ resistor.
REmember to place components as close ti the GPU as possible.

R8636 is reserved for Metal Xtal

SPEC. (DG-05587-001_v03_p.162)
Adding a pull down to the DACA_VDD with a 10kΩ resistor to GND.
All other DAC I/O pins (including DACA_VREF, DACA_REST)
can be left floating.





SPEC. (DG-05587-001_v03_p.191_Table 102)
Multi_Strap_Ref0_GND 40.2kΩ 1% to GND

L3	(DA-05691-001_v04_p.3_Table 2)
N13P-GL	10kΩ pull-up to 3.3V
N13M_GE1	NC
N13M-GS	NC
N13P-GS	NC

TABLE VIDEO MEMORY

	HYNIX 128Mx16 0110	SAMSUNG 128Mx16 0111	HYNIX 64Mx16 0010	Samsung 64Mx16 0011
900MHz	72.52G63.A0U 1-007155	72.42164.D0U 1-007156	72.51G63.H0U 1-007157	72.41164.Q0U 1-007356
ROM_SI PD R8627	34.8Kohm 64.34825.6DL	45.3Kohm 64.45325.6DL	15Kohm 64.15025.6DL	20Kohm 64.20025.6DL

The GB4-128 package is available in a 29 mm × 29mm footprint.
128-bit memory interfaces respectively.

Recommended NVVDD Voltage Regulator Phase Coount

GPU SKU	Phase Count Target
N13M-GE1	Single phase
N13M-GS	Two phase
N13P-GL	Two phase
N13P-GS	Two phase

29 x 29 PACKAGE
V: N13P-GS/GL (25~30W)
B: N13M-GS/GE (15~20W)

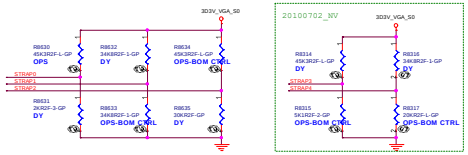
128Mx16:

hynix - H5TQ2G63BFR-11C
Samsung - K4W2G1646C-HC11

64Mx16:

Hynix - H5TQ1G63DFR-11C
Samsung - K4W1G1646G-BC11

	TABLE NVIDIA	N12P-GE DEV ID: 0xDF5 0101	N12P-GV DEV ID: 0x0DF7(ES)	N12M-GE DEV ID: 0xA7A 1010
STRAP1	R8632	DY	DY	35Kohm 64.34825.6DL
	R8633	35Kohm 64.34825.6DL	35Kohm 64.34825.6DL	DY
STRAP2	R8634	DY	45Kohm 64.45325.6DL	15Kohm 64.15025.6DL
	R8635	30Kohm 64.30025.6DL	DY	DY



<Core Design>
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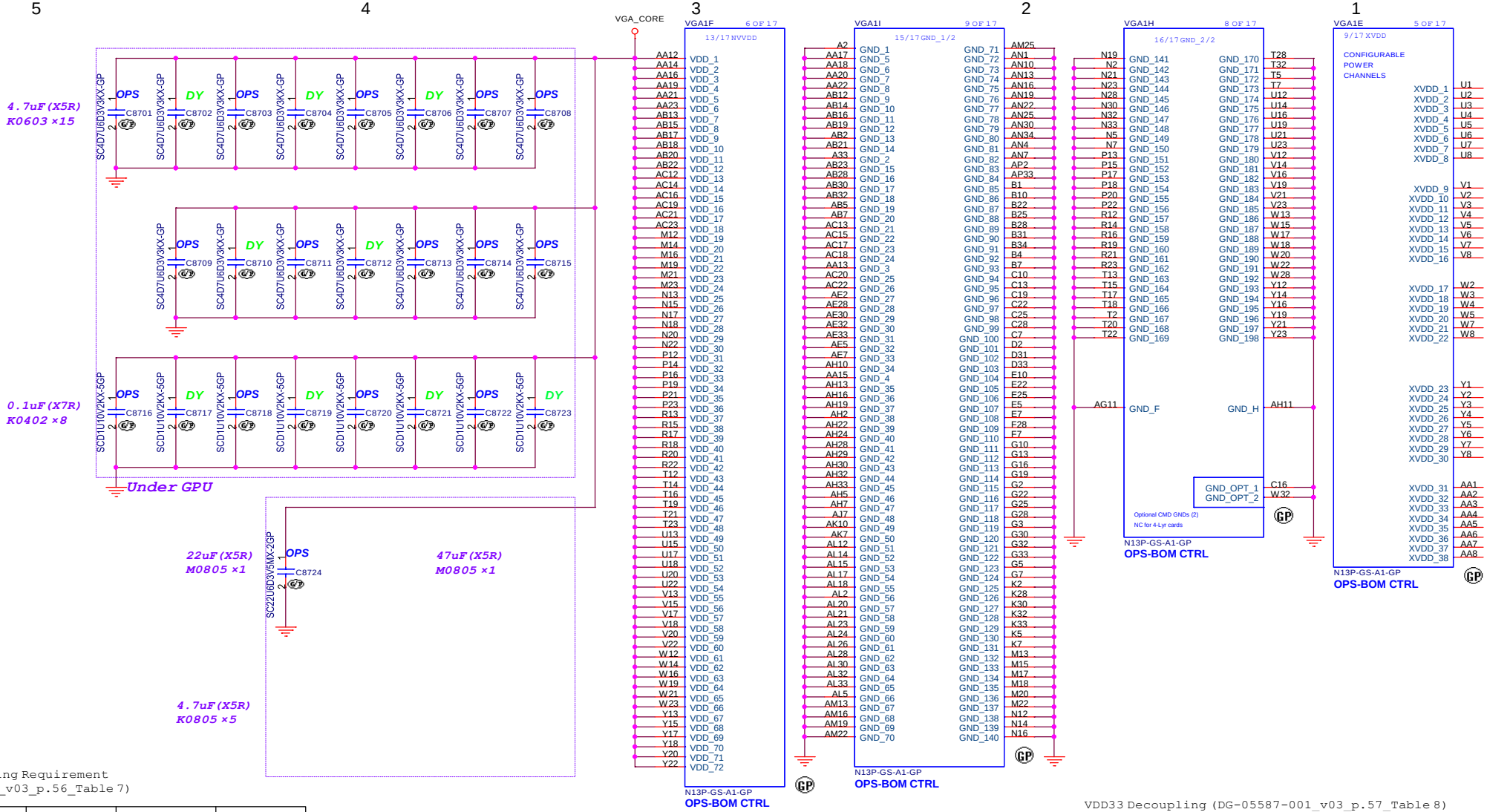
Taipei Hsien 221, Taiwan, R.O.C

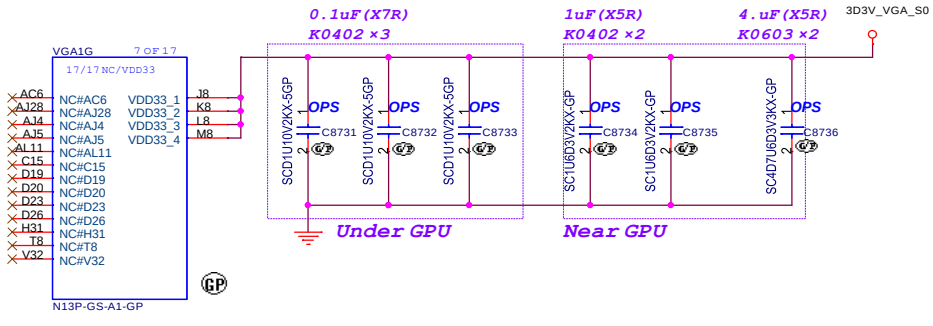
Title: N13P_GPU (4/5): GPIO/STRAP
Size: A1 | Document Number: LA48 | Rev: SD
Date: Friday, January 06, 2012 | Sheet 86 of 103



NVVDD Decoupling Requirement
(DG-05587-001_v03_p.56_Table 7)

Capacitor Type	Footprint		Population	Location
4.7uF	X6S	0603	15	10	Under GPU
0.1uF	X7R	0402	8	4	Under GPU
47uF	X5R	0805	1	1	Near GPU
22uF	X5R	0805	1	1	Near GPU
4.7uF	X5R	0805	5	5	Near GPU

X7R (+/-15%, -55~125°C
X6S (+/-22%, -55~105°C
X5R (+/-15%, -55~85°C



VDD33 Decoupling (DG-05587-001_v03_p.57_Table 8)

Capacitor Type	Footprint		Population	Location
0.1uF	X7R	0402	3	3	Under GPU
1uF	X5R	0402	2	2	Near GPU
4.7uF	X5R	0603	1	1	Near GPU

X7R (+/-15%, -55~125°C
X5R (+/-15%, -55~85°C

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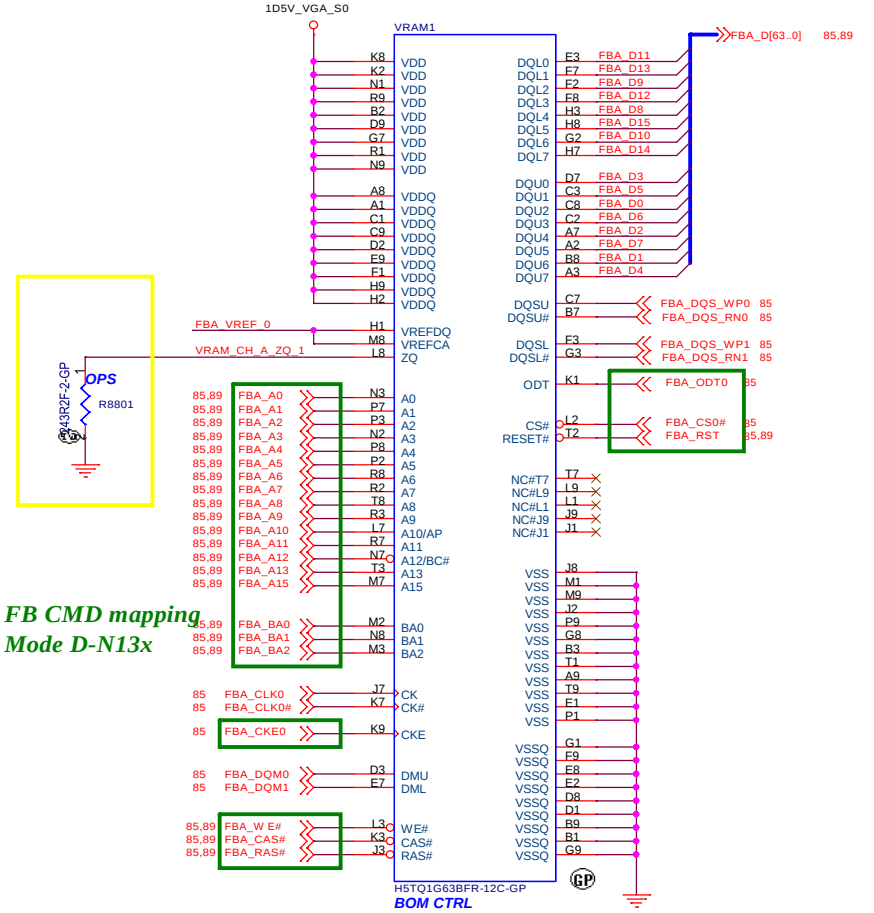
Taipei Hsien 221, Taiwan, R.O.C

Title: N13P_GPU (5/5): PWR/GND

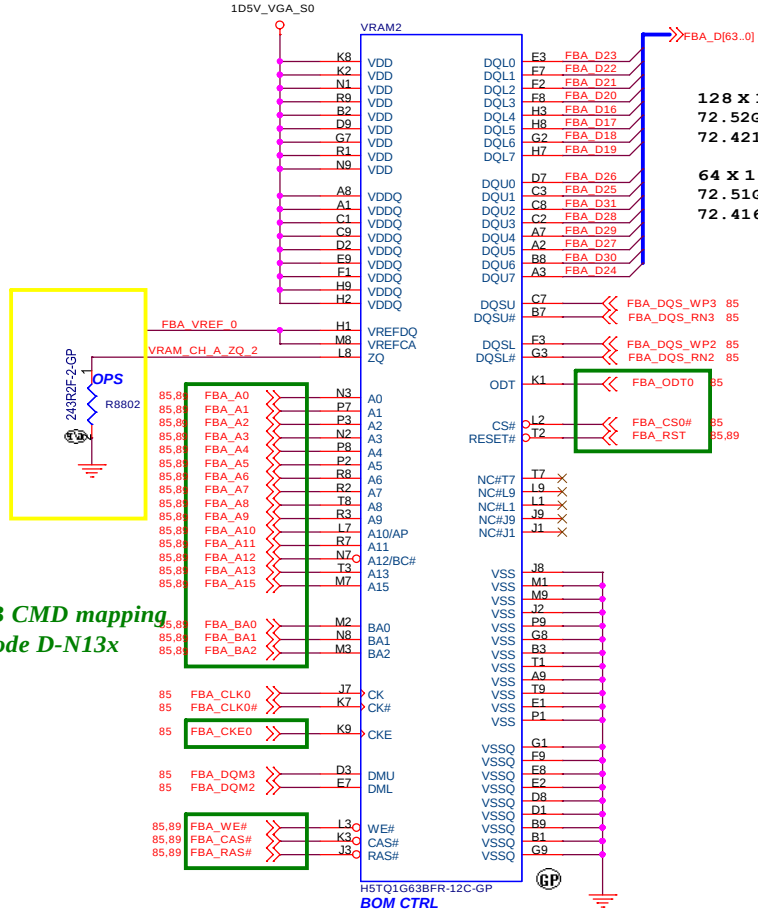
Size: A3 | Document Number: LA48 | Rev: SD

Date: Friday, January 06, 2012 | Sheet 87 of 103

VIDEO FRAME BUFFER PORT A



FB CMD mapping
Mode D-N13x



FB CMD mapping
Mode D-N13x

128 X 16
72.52G63.A0U
72.42164.D0U IC VRAM K4W2G1646C-HC11 FBGA96

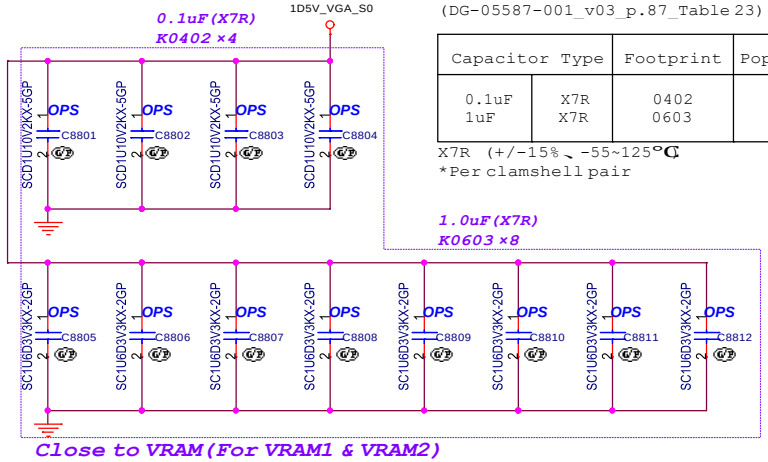
64 X 16
72.51G63.H0U IC VRAM H5TQ1G63DFR-11C FBGA 96BALLS
72.41646.Q0U IC VRAM K4W1G1646G-BC11 FBGA 96BALLS

128Mx16:

hynix – H5TQ2G63BFR-11C
Samsung – K4W2G1646C-HC11

64Mx16:

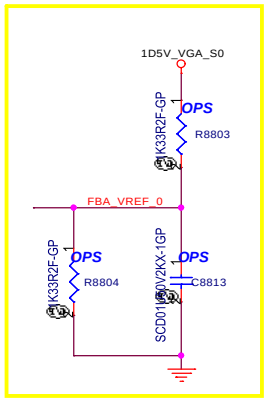
Hynix – H5TQ1G63DFR-11C
Samsung – K4W1G1646G-BC11



Combined Memory FBVDD/Q Decoupling DDR3×16 with Clamshell Layout
(DG-05587-001_v03_p.87_Table 23)

Capacitor Type		Footprint	Population	Location
0.1uF	X7R	0402	4	Close to VRAM
1uF	X7R	0603	8	Close to VRAM

X7R (+/-15%、-55~125℃)
*Per clamshell pair



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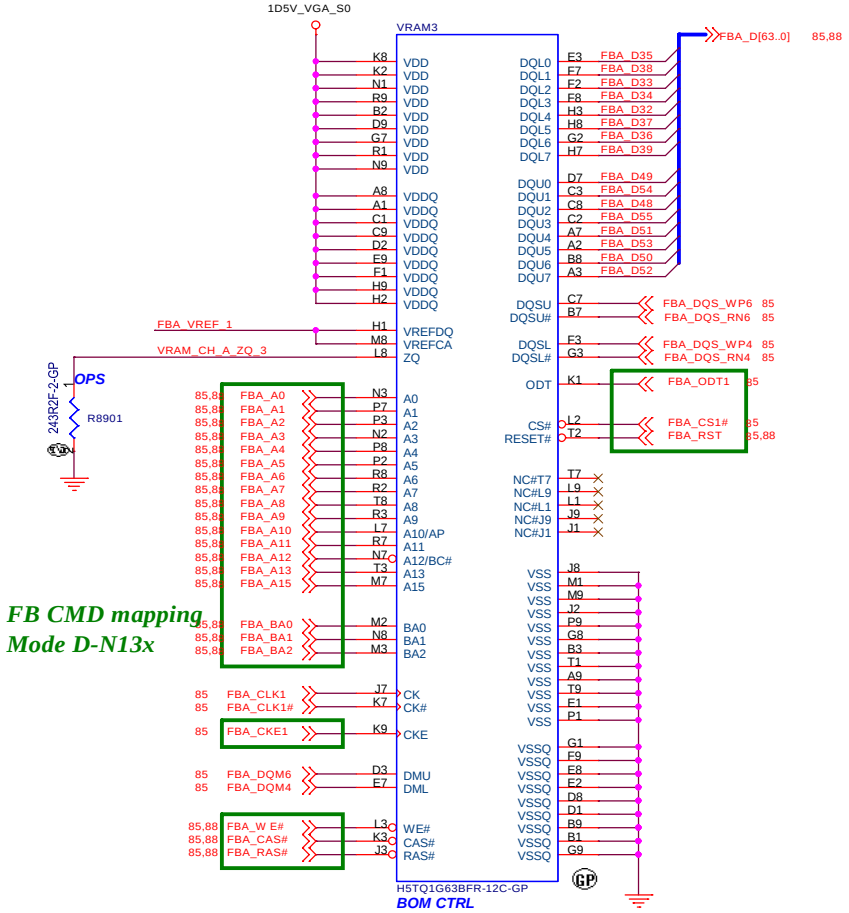
Taipei Hsien 221, Taiwan, R.O.C.

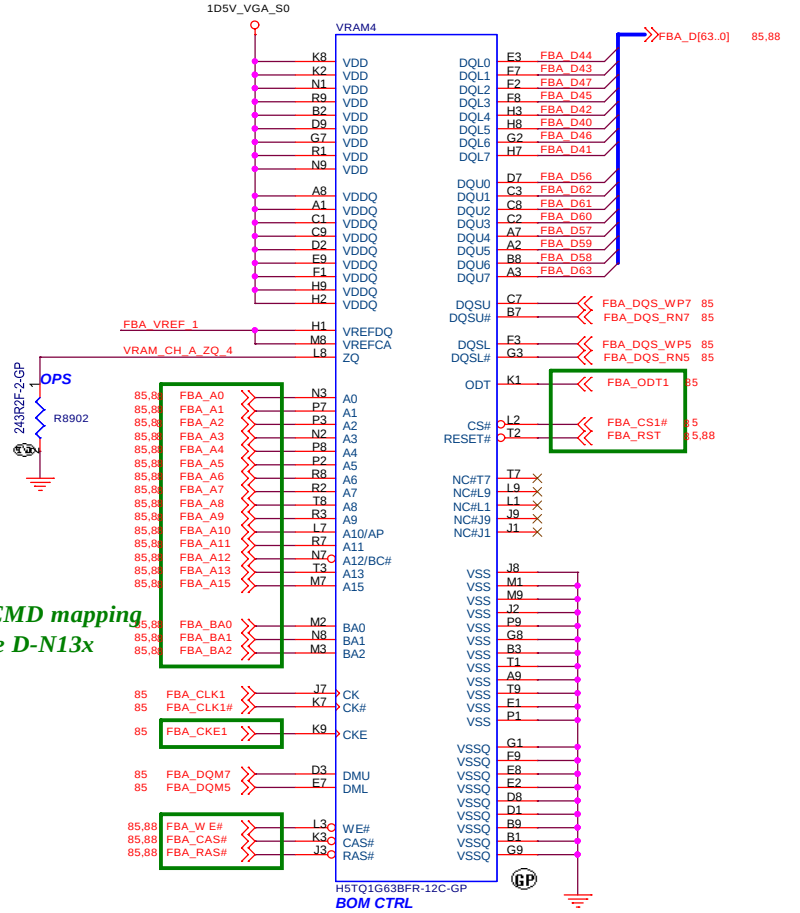
Title: **CHANNEL-A_VRAM1,2 (1/4)**

Size: A3 | Document Number: **LA48** | Rev: **SD**

Date: Friday, January 06, 2012 | Sheet 88 of 103

VIDEO FRAME BUFFER PORT A

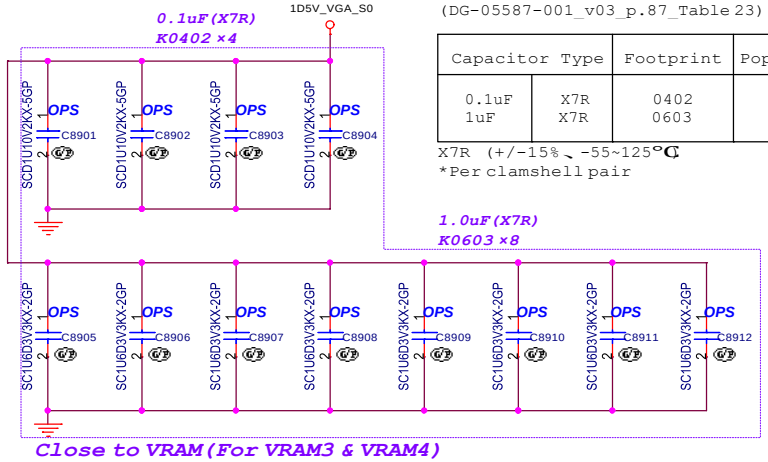


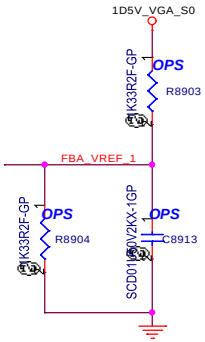


Combined Memory FBVDD/Q Decoupling DDR3×16 with Clamshell Layout
(DG-05587-001_v03_p.87_Table 23)

Capacitor Type		Footprint	Population	Location
0.1uF	X7R	0402	4	Close to VRAM
1uF	X7R	0603	8	Close to VRAM

X7R (+/-15%、-55~125℃)
*Per clamshell pair





<Core Design>

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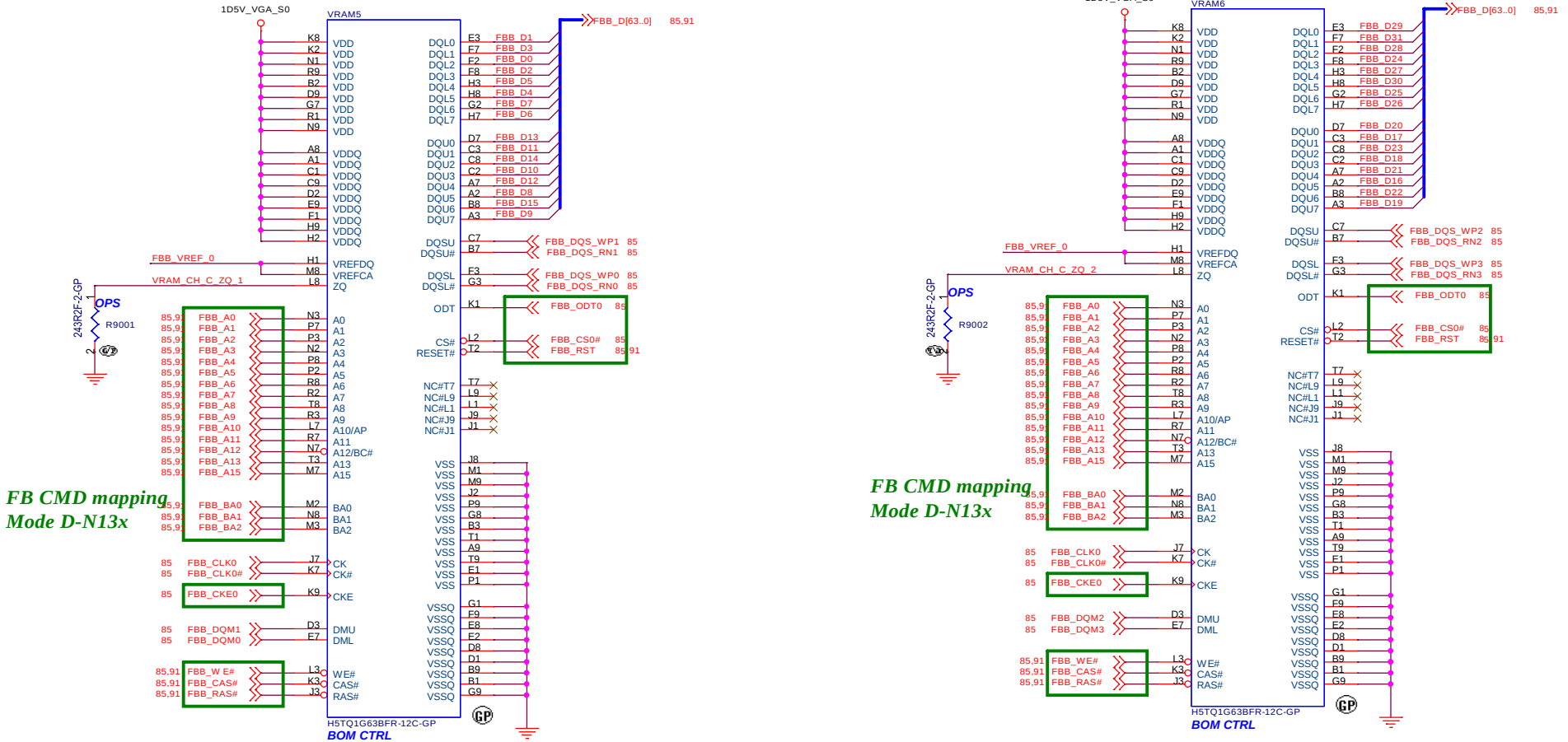
Title: CHANNEL-A_VRAM3,4 (2/4)

Size: A3 | Document Number: LA48 | Rev: SD

Date: Friday, January 06, 2012 | Sheet 89 of 103

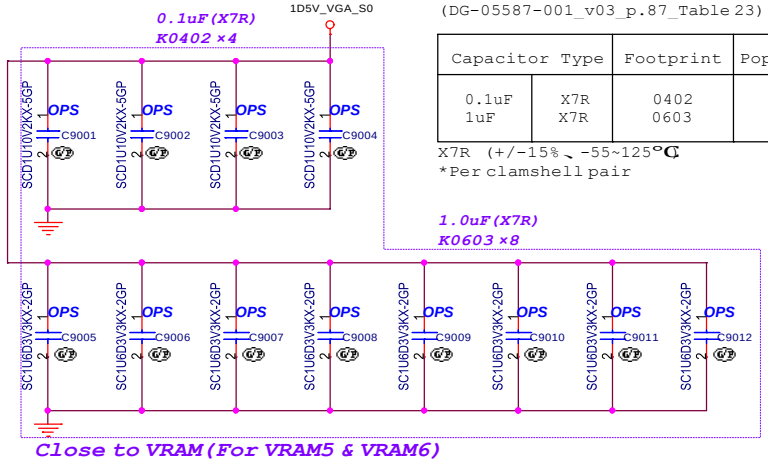
VIDEO FRAME BUFFER PORT C

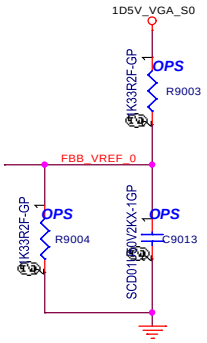


Combined Memory FBVDD/Q Decoupling DDR3×16 with Clamshell Layout
(DG-05587-001_v03_p.87_Table 23)

Capacitor Type		Footprint	Population	Location
0.1uF	X7R	0402	4	Close to VRAM
1uF	X7R	0603	8	Close to VRAM

X7R (+/-15%、-55~125℃)
*Per clamshell pair





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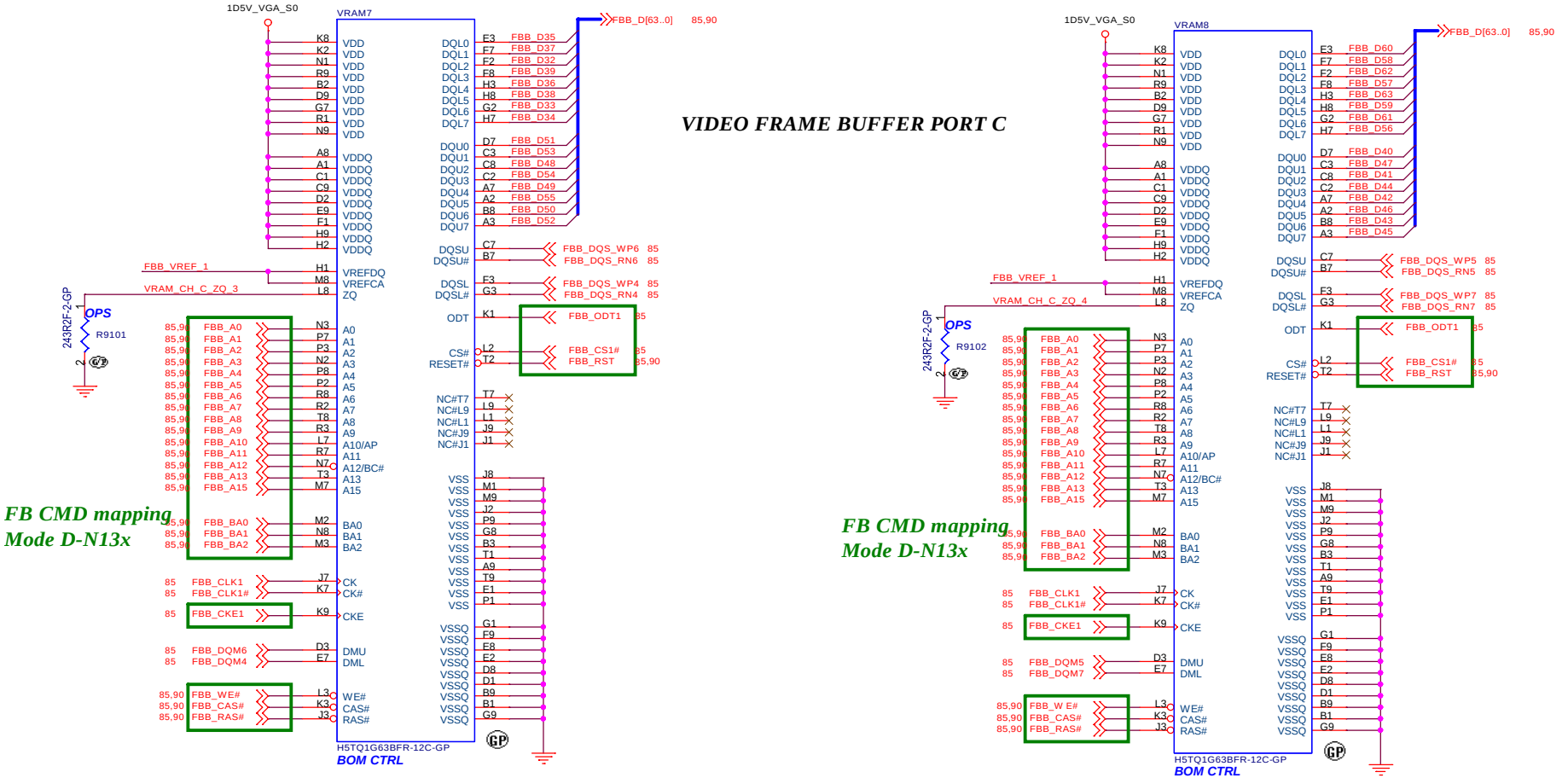
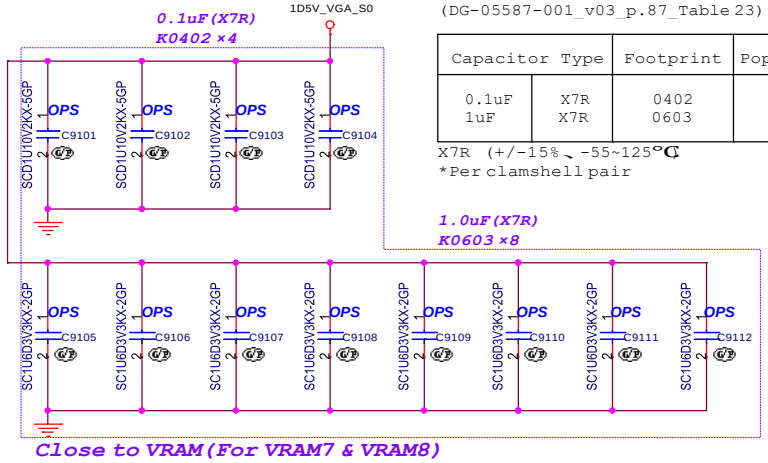
Title	CHANNEL-C_VRAM5,6 (3/4)	
Size A3	Document Number LA48	Rev SD
Date: Friday, January 06, 2012	Sheet 90 of 103	



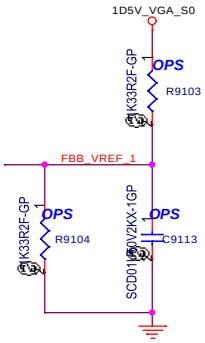
VIDEO FRAME BUFFER PORT C



Combined Memory FBVDD/Q Decoupling DDR3×16 with Clamshell Layout
(DG-05587-001_v03_p.87_Table 23)

Capacitor Type		Footprint	Population	Location
0.1uF	X7R	0402	4	Close to VRAM
1uF	X7R	0603	8	Close to VRAM

X7R (+/-15%、-55~125℃)
*Per clamshell pair



<Core Design>

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Title	CHANNEL-C_VRAM7,8 (4/4)	
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SSID = PWR.Plane.Regulator_GFX

	Main source	2nd source
PU9202	84.03606.037 FDMS3606S-GP-U	
PU9206	84.03606.037 FDMS3606S-GP-U	

BOM control

		N13P-GS 71.0N13P.00U	N13P-GL 71.0N13P.B0U	N13M-GS 71.0N13M.E0U	N13M-GE1 71.0N13M.C0U
NVVDD Boot Voltage		0.9V VID[6:0]=0110000	0.975V VID[6:0]=0101010	0.9V VID[6:0]=0110000	0.875V VID[6:0]0110010
NV_VID1	PR9215	DY	63.10334.1DL	DY	63.10334.1DL
	PR9230	63.10334.1DL	DY	63.10334.1DL	DY
NV_VID3	PR9217	DY	63.10334.1DL	DY	DY
	PR9232	63.10334.1DL	DY	63.10334.1DL	63.10334.1DL
NV_VID4	PR9218	63.10334.1DL	DY	63.10334.1DL	63.10334.1DL
	PR9233	DY	63.10334.1DL	DY	DY

Q1: Id=11A, Qg=10~14nC,
Rdson=7.5~9.8 mohm
Q2: Id=23A, Qg=27~38nC,
Rdson=1.7~2.1 mohm

Panasonic. 0.36uH 10*11.5*4
DCR=1.1mohm
Idc=17A, Isat=24A

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Title: TPS51728_VGA_CORE

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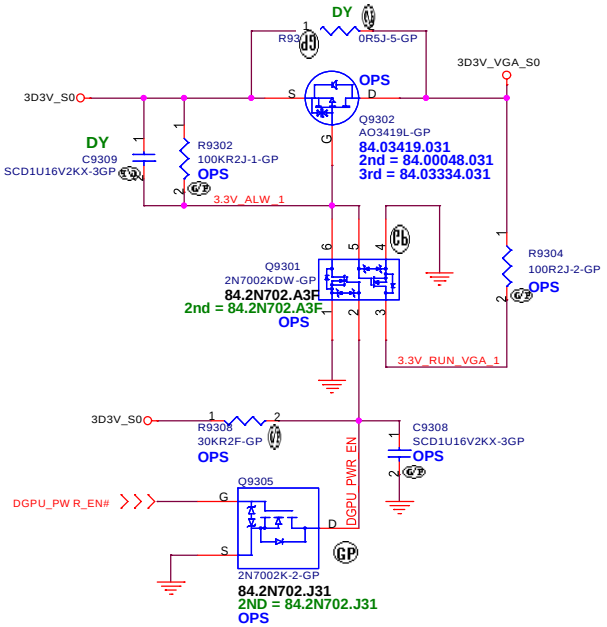
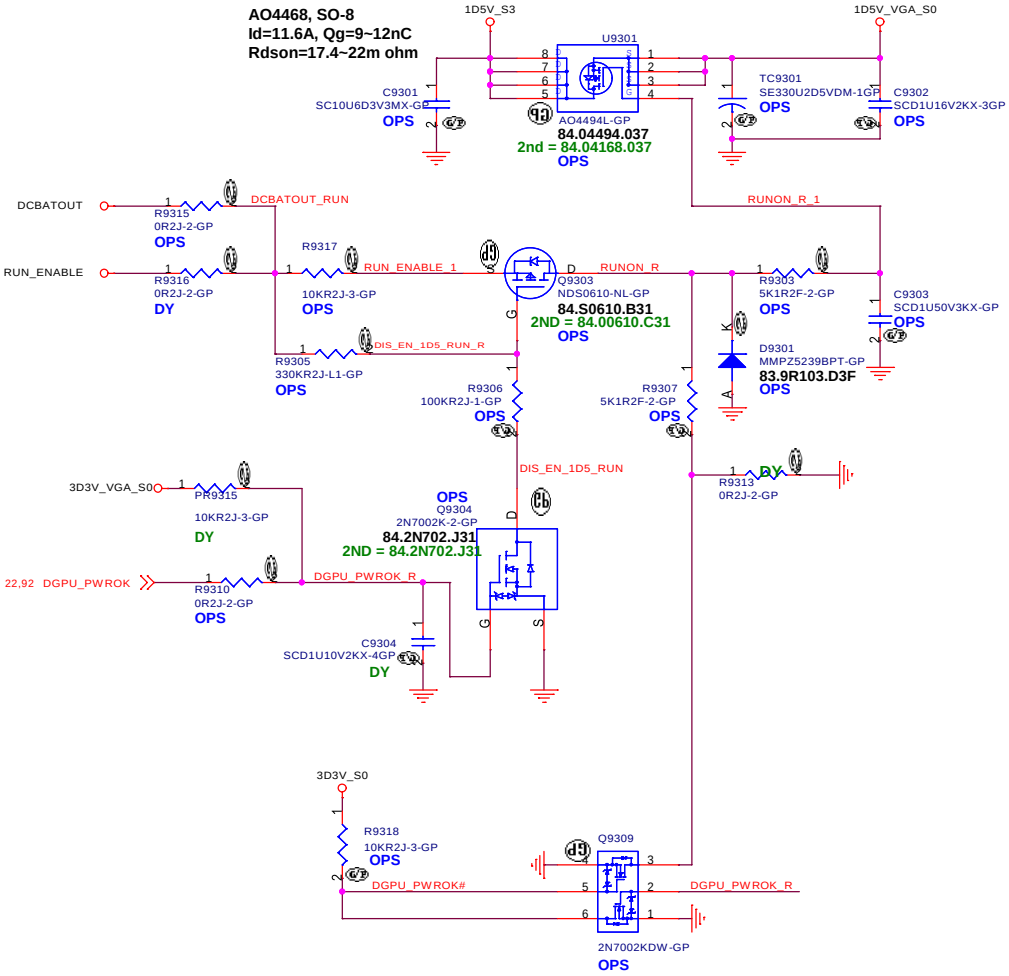
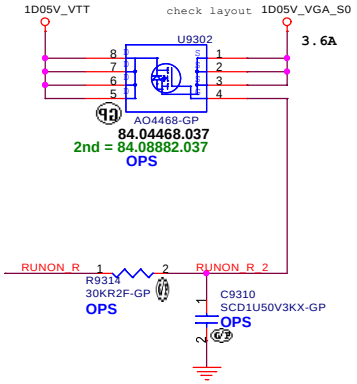
+3VS to 3.3V_DELAY Transfer

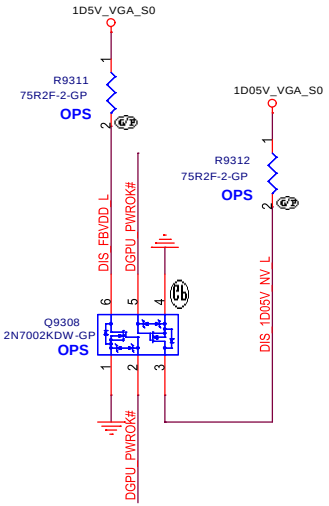


1D5V_VGA_S0



1.05V to 1.05V_VGA_S0 Transfer





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Title: DISCRETE VGA POWER		
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緯創資通

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Title: <Title>		
Size: A4	Document Number: LA480	Rev: SD
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<Core Design>

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Title: ***Reserved***

Size	Document Number	Rev
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Title

TOUCH PANEL

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CPU Plate

H14 HOLET157B276R134-GP ZZ.SCREW.091
H15 HOLET157B276R134-GP ZZ.SCREW.091
H16 HOLET157B276R134-GP ZZ.SCREW.091
H17 HOLET157B276R134-GP ZZ.SCREW.091

VGA Std-Off

H1 STF237R128H42-1-GP 34.4GD01.001
H2 STF237R128H42-1-GP 34.4GD01.001
H21 STF237R128H42-1-GP 34.4GD01.001

MINI PCIE

H18 STF256R89H178-GP 34.4B417.001

DCBATOUT
EC9729 EC9727 EC9728 SCD1U25V2KX-GP
VCCSA
EC9730 SC1KP50V2KX-1GP
DY EC9731 EC9732 EC9733 SCD1U25V2KX-GP

XDP_DBRESET# 5,19
H_CPUPWRGD 5,22
PLT_RST# 5,18,27,31,36,65,66,71,80,82,83

14" Structure boss

H3 HOLE256R115-GP ZZ.00PAD.D11
H4 HOLE256R115-GP ZZ.00PAD.D11
H5 HOLE315X315R91-S1-GP ZZ.00PAD.581
H7 HOLE355X355R111-S1-GP ZZ.00PAD.571
H8 HOLE335R115-GP ZZ.00PAD.D01
H10 HOLE237R95-GP ZZ.00PAD.921
H11 HOLE237R95-GP ZZ.00PAD.921
H12 HOLE335R115-GP ZZ.00PAD.D01
H13 HOLE237R95-GP ZZ.00PAD.921
H19 HOLE315R95-GP ZZ.00PAD.911

DCBATOUT
EC9705 EC9706 EC9707 EC9708 EC9709 EC9710 EC9711 EC9712 EC9713 EC9714 SCD1U25V2KX-GP
3D3V_S0_CAMERA
EC9715 SCD1U25V2KX-GP
3D3V_AUX_S5
EC9716 SCD1U25V2KX-GP
3D3V_AUX_KBC
EC9717 SCD1U25V2KX-GP
3D3V_VGA_S0
EC9718 SCD1U25V2KX-GP
ODD_PWR_5V
EC9719 SCD1U25V2KX-GP
VCC_CORE
EC9720 EC9721 SCD1U25V2KX-GP
5V_S5
EC9722 EC9723 EC9724 SCD1U25V2KX-GP

3D3V_S0
R9704 100R2J-2-GP DY
3D3V RUNPWR
Q9704 2N7002A-7-GP DY
PS_S3CNTRL

5V_S0
R9705 100R2J-2-GP DY
5V RUNPWR
Q9705 2N7002A-7-GP DY
PS_S3CNTRL

5V_USB2_S3
EC9725 SCD1U25V2KX-GP
5V_USB1_S3
EC9726 SCD1U25V2KX-GP

1D05V_VTT
R9701 100R2J-2-GP DY
VTT RUNPWR
Q9701 2N7002A-7-GP DY
36,37 PS_S3CNTRL
PS_S3CNTRL

VCC_CORE
R9706 100R2J-2-GP DY
CORE RUNPWR
Q9706 2N7002A-7-GP DY
PS_S3CNTRL

VCC_GFXCORE
R9707 100R2J-2-GP DY
GFX RUNPWR
Q9707 2N7002A-7-GP DY
PS_S3CNTRL

VCCSA
R9709 100R2J-2-GP DY
1D05V RUNPWR
Q9709 2N7002A-7-GP DY
PS_S3CNTRL

1D8V_S0
R9702 100R2J-2-GP DY
1D8V RUNPWR
Q9702 2N7002A-7-GP DY
PS_S3CNTRL

AD+
EC9702 EC9703 EC9704 SCD1U25V2KX-GP

For Discharge

3D3V_S5
R9710 100KR2J-1-GP DY
PM_SLP_S4
Q9710 2N7002A-7-GP DY
19,27,46 PM_SLP_S4#

1D5V_S3
R9711 100R2J-2-GP DY
1D5V RUNPWR
Q9711 2N7002A-7-GP DY

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Title: UNUSED PARTS/EMI Capacitors
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<Core Design>

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Title: ***Change History***

Size	Document Number	Rev
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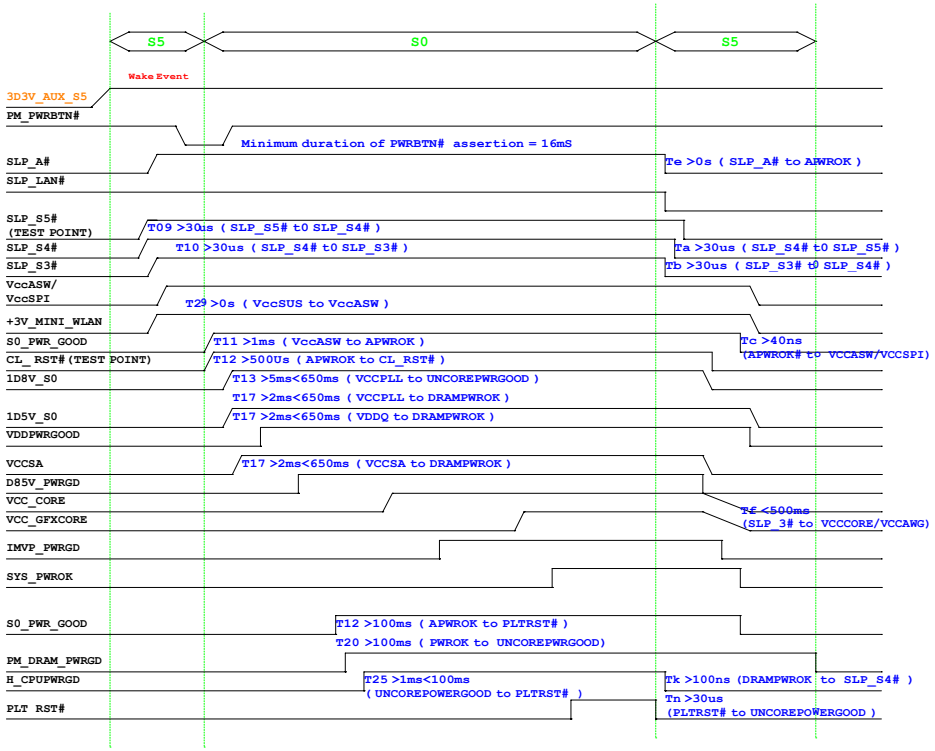
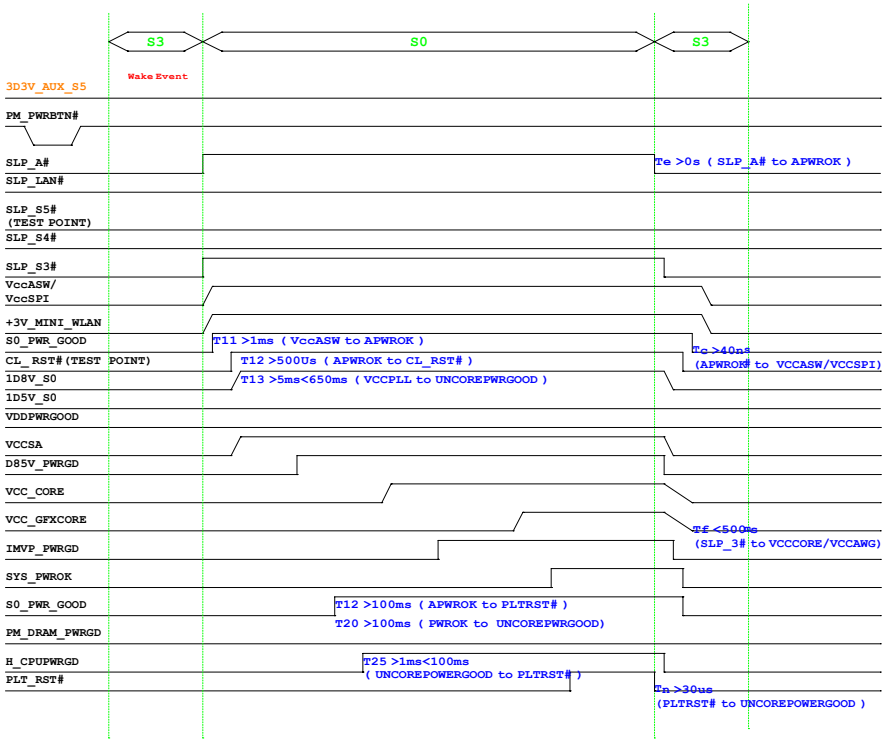
Intel-Power Sequence

(S5-to-S0-to-S5)



Intel PCH Pin Name	Main board PCH Pin Name
VccSUS (5V/3V)	3D3V_AUX_S5
PWRBTN#	PM_PWRBTN#
SLP_A#	SLP_A#
SLP_LAN#	SLP_LAN#
SLP_S5#	PM_SLP_S5#
SLP_S4#	PM_SLP_S4#
SLP_S3#	PM_SLP_S3#
VccASW/ VccSPI	VccASW/ VccSPI
Vcc_WLAN	+3V_MINI_WLAN
PWROK/APWROK	S0_PWR_GOOD
CL_ RST#	CL_ RST#
VCCPLL	1D8V_S0
VDDQ	1D5V_S0
VR_VDDQPWRGOOD	VDDPWRGOOD
VCCSA	VCCSA
IMVP7_VR_EN	D85V_PWRGD
VccCore	VCC_CORE
VccAXG	VCC_GFXCORE
IMVP7_PWRGD	IMVP_PWRGD
SYS_PWROK	SYS_PWROK
PWROK	S0_PWR_GOOD
DRAMPWROK	PM_DRAM_PWRGD
UNCOREPWRGOOD	H_CPUPWRGD
PLTRST#	PLT_RST#

(S3-to-S0-to-S3)



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Title: Change History

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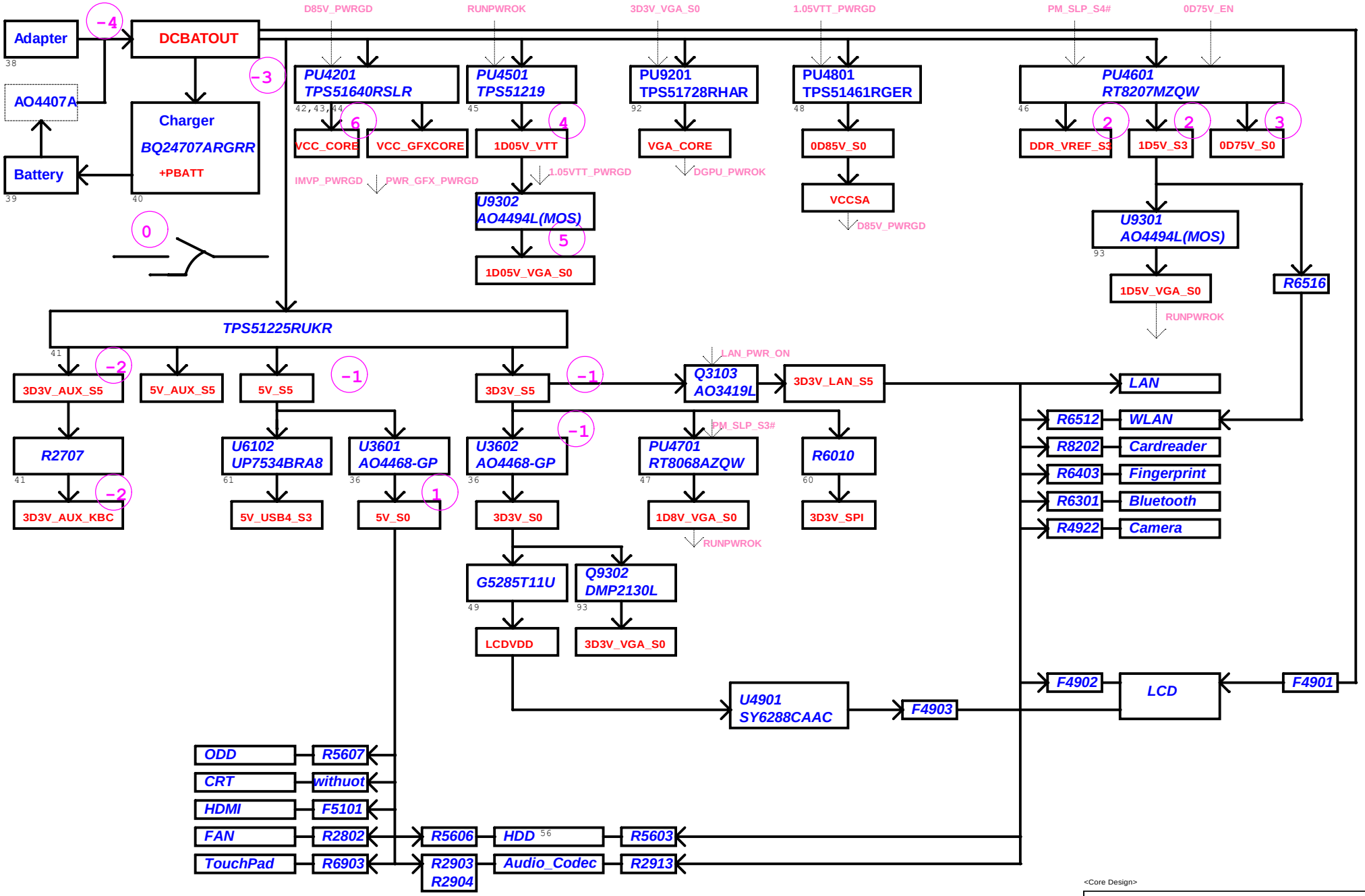

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Title: Power Block Diagram

Size	Document Number	Rev
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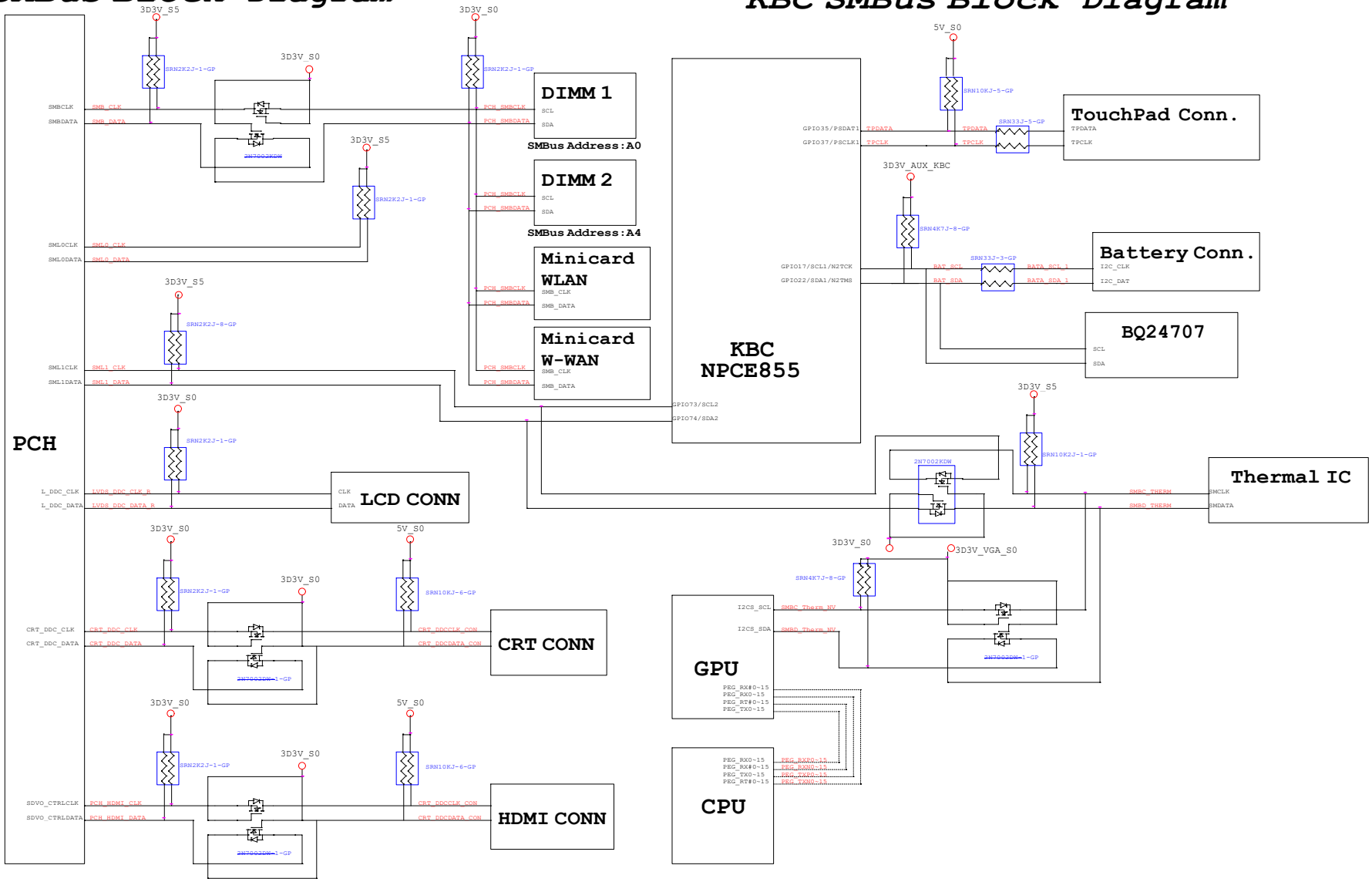
PCH SMBus Block Diagram



KBC SMBus Block Diagram

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Title: SMBUS Block Diagram

Size: A2 | Document Number: LA480 | Rev: SD

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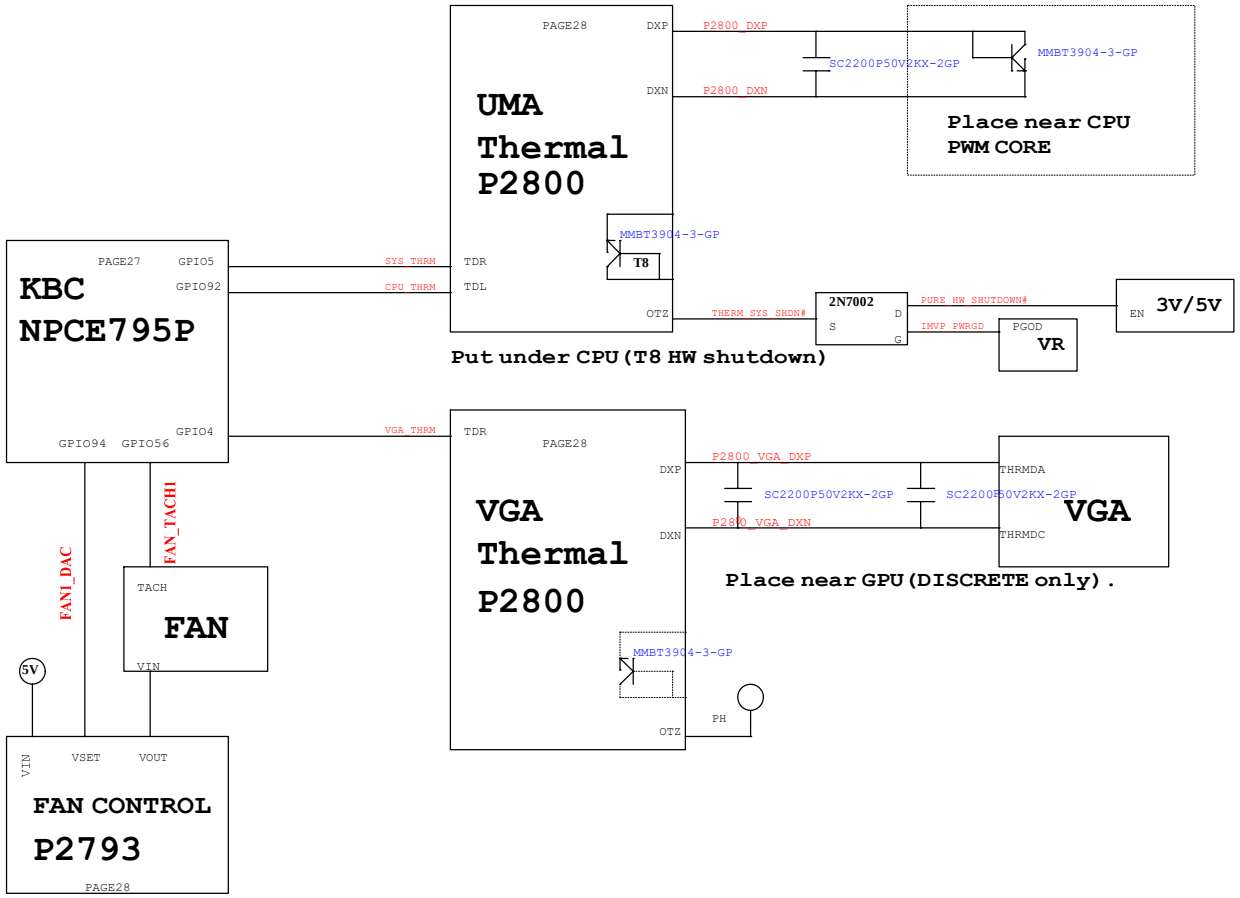
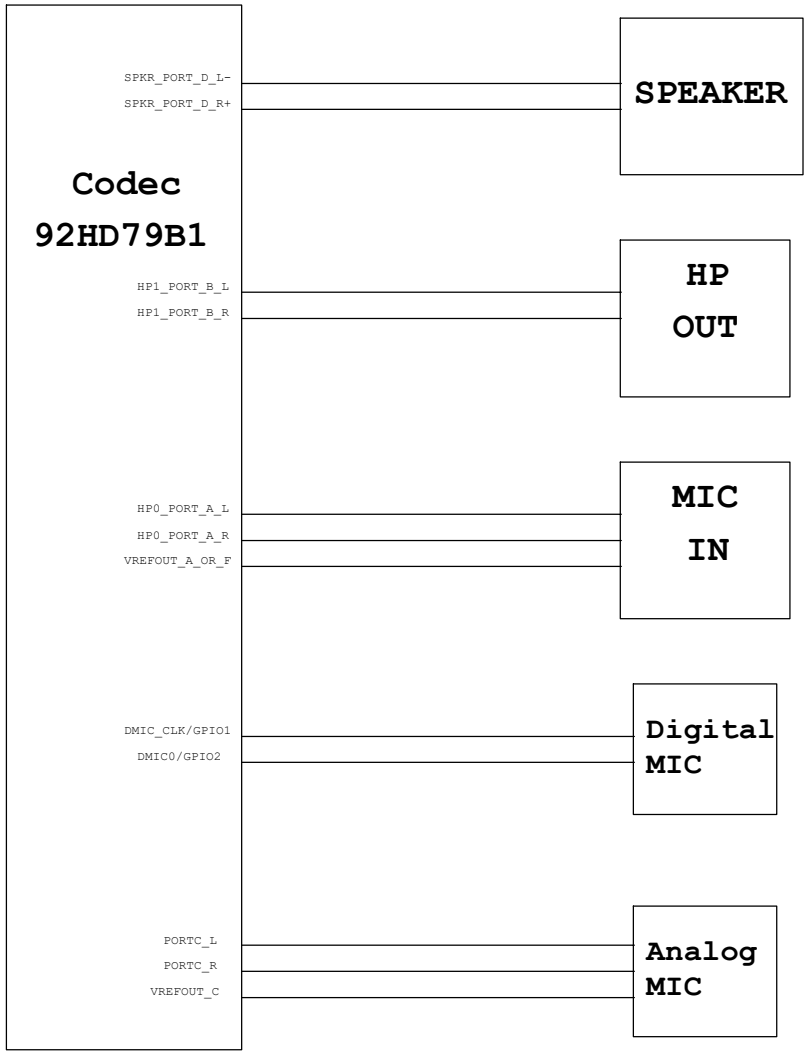
Thermal Block Diagram



Audio Block Diagram



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Title: Thermal/Audio Block Diagram

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Title: ***Change History***

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